TECHNICAL MANUAL
FOR
ERROR RATE TEST SET
MODEL KS-20775, L2

MANUFACTURED BY:

Bowmar/ALI, Incorporated
531 Main Street
Acton, Massachusetts U.S.A. 01720

Rev. G
January 1981

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Bowmar

Communications
Test
Equipment

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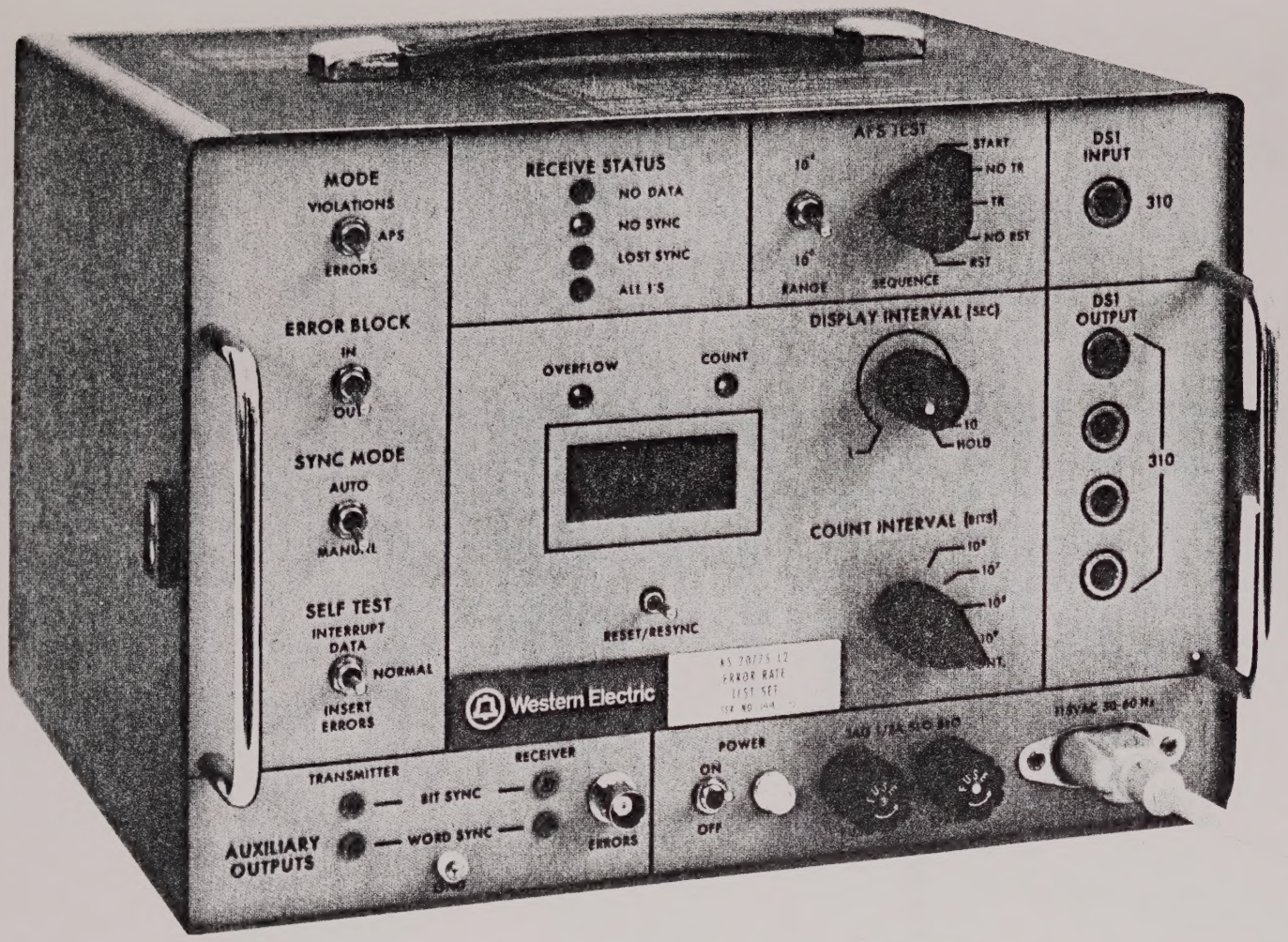

PHOTOGRAPH OF KS-20775 L2

ERROR RATE TEST SET

CONTENTS

CHAPTER 1		INTRODUCTION
	1.1	Description
	1.2	Scope
	1.3	Specification Summary
CHAPTER 2		INSTALLATION AND SELF TEST
	2.1	Preparation
	2.2	Checkout/Self Test Procedure
CHAPTER 3		OPERATION AND APPLICATIONS
	3.1	Controls, Indicators, and Connectors
	3.2	Applications
CHAPTER 4		DESCRIPTION OF FUNCTIONS
	4.1	General
	4.2	Transmitter Circuits
	4.3	Receiver
CHAPTER 5		MAINTENANCE
	5.1	General
	5.2	Test Equipment Requirements
	5.3	Calibration Procedure
	5.4	Performance Checks
	5.5	Troubleshooting
CHAPTER 6		DIAGRAMS
CHAPTER 7		PARTS AND MANUFACTURERS

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1.0 INTRODUCTION

1.1 Description

The Bowmar/ALI KS-20775, L2 Error Rate Test Set is a lightweight, portable instrument capable of performing a reliable check of T1 lines and T1 automatic protection switches (APS). The Test Set is well-suited for checkout of T1 to T2 (M12) multiplexers, T1 to L-carrier modems, and similar digital transmission equipment.

This instrument provides two basic test techniques. The first is achieved by injecting a repeating pattern of data bits from the Test Set's Transmitter section to a system under test, then monitoring the system's output with a Receiver section from the same or a second Test Set. The Test Set's Receiver section may be set to monitor either logical errors or bipolar violations. A tally of these errors or violations, as detected over a selected interval of time, is then presented on the Test Set's numerical display. In the second technique, the Test Set intercepts the random bipolar data and adds violations at error rates required to test the transfer and to reset the threshold of an automatic protection switch.

1.2 Scope

This manual contains descriptive details of the Error Rate Test Set plus related applications notes, maintenance information, diagrams, and parts information. The descriptive details are reduced to categories of physical and functional specifications, operating procedures, and operating principles. The manual's purpose is to provide sufficient familiarization to enable effective use and proper maintenance of the Test Set.

1.3 Specification Summary

Output Pattern:	A 1,048,575 bit quasi-random pattern limited to 14 consecutive zeros; compatible with Western Electric J98710R Quasi-Random Signal Source.
Input:	Balanced; one jack which accepts a WE 310-type plug (T & R).
Outputs:	A. Main: balanced; four jacks which accept WE 310-type plugs (T & R).
	B. Auxiliary: unbalanced; a GND (ground) terminal, a BNC connector for ERRORS output, and four pin jacks

which allow monitoring of the signals listed below.

1. TRANSMITTER BIT SYNC
2. TRANSMITTER WORD SYNC
3. RECIEVER BIT SYNC
4. RECEIVER WORD SYNC

Controls:

MODE Switch — 3-position:
1. VIOLATIONS
2. APS
3. ERRORS

ERROR BLOCK Switch — 2-position:
1. IN
2. OUT

SYNC MODE Switch — 2-position:
1. AUTO
2. MANUAL

SELF TEST Switch — 3-position:
1. INTERRUPT DATA (momentary)
2. NORMAL
3. INSERT ERRORS (momentary)

APS TEST Switches

A. RANGE: 2-position
1. 10^{-4}
2. 10^{-6}

B. SEQUENCE: 5-position
1. START
2. NO TR
3. TR
4. NO RST
5. RST

DISPLAY INTERVAL (SEC) Control: 1 to 10 seconds, plus a detent setting for HOLD.

COUNT INTERVAL (BITS) Switch: 5-position:
1. 10^{6}
2. 10^{7}
3. 10^{8}
4. 10^{9}
5. CONT

RESET/RESYNC Switch: Momentary toggle.

POWER Switch: 2-position:
1. ON
2. OFF

Indicators

RECEIVE STATUS Indicators:	4 separate indicators; solid state: 1. NO DATA 2. NO SYNC 3. LOST SYNC 4. ALL 1's
Display Status Indicators:	2 separate indicators; solid state; 1. OVERFLOW 2. COUNT
Display:	3-digit; solid state.
FUSE and SPARE:	1 each; 3AG, 1/2 A, slow blow
Power Source:	115 Vac ±10%, 50 to 60 Hz, single phase.
Receiver Input Threshold:	0.2 to 5.0 V peak
Sync. Acquisition Time:	Less than 200 clock pulses. (Test Set will not resync on isolated error bursts of less than 6 consecutive errors).
Transmitter Output Bipolar Pulse Characteristics	
Height of output pulse:	3 V ±0.3 V
Unbalance in height of negative and positive pulse:	0.15 V
Width of output pulse (half amplitude)	324 ±30 nsec
Unbalance in width of negative and positive pulse:	±15 nsec
Maximum rise or fall time:	80 nsec
Overshoot at trailing edge of pulse:	10 to 30% of pulse height with decay to 10% or less of base line-to-peak value within 400 nsec.
Auxiliary Outputs:	4 pin jacks 1 BNC Connector 1. TRANSMITTER BIT SYNC 2. TRANSMITTER WORD SYNC 3. RECEIVER BIT SYNC 4. RECEIVER WORD SYNC 5. ERRORS (BNC CONNECTOR)
Operating Environment:	0 to 50°C (32 to 120°F) to 95% relative humidity.

2.0 INSTALLATION AND SELF TEST

2.1 Preparation

2.1.1 Remove the Error Rate Test Set from its shipping container.

2.1.2 Remove the front cover.

2.1.3 Check for the presence of 3AG, 1/2A, slow blow fuses.

2.1.4 Remove the power cord from the front cover and connect the Test Set to a 115 V ac, 50-60 Hz, single-phase power source.

2.1.5 Set the POWER switch to ON and note whether or not the indicator illuminates.

2.2 Check/Self Test Procedure

Follow the procedure outlined below.

2.2.1 Set switches to the following initial positions:

MODE	-to VIOLATIONS
ERROR BLOCK	-to OUT
SYNC MODE	-to MANUAL
SELF TEST	-to NORMAL
DISPLAY INTERVAL (SEC)	-to '1' (full counterclockwise)
COUNT INTERVAL (BITS)	-to '10^6'
RESET/RESYNC	-to Momentarily Actuate and Release

2.2.2 Observe indicators for the following initial responses:

NO DATA	-off
NO SYNC	-on
LOST SYNC	-on
All 1's	-off
OVERFLOW	-off
COUNT	-alternately on for approximately 2/3 second, off for approximately 1 second.
DISPLAY	-'000' (constant)

2.2.3 Turn the DISPLAY INTERVAL (SEC) control clockwise to the '10' position. The COUNT indicator should alternately be on for approximately 2/3 second and off for approximately 10 seconds.

2.2.4 Place the DISPLAY INTERVAL (SEC) control in its HOLD (detent) position and momentarily operate the RESET/RESYNC switch. The COUNT indicator should come on for approximately 2/3 second and then remain off indefinitely. Check the off condition for at least twenty seconds.

2.2.5 Place the DISPLAY INTERVAL (SEC) control at some point between '1' and '5'. Hold the SELF TEST switch at its INSERT ERRORS position. The count on the Display should change by increments of two from a starting count of '000' to a final count of '008' while the COUNT indicator is on. At the count of '008', the Display should hold for the period set by the DISPLAY INTERVAL (SEC) control, then it should clear to '000' and begin a new cycle. The first count interval may not yield a total of eight errors, but each succeeding interval should register a count of '008' on the Display.

2.2.6 Holding the SELF TEST switch at its INSERT ERRORS position, change the COUNT INTERVAL (BITS) switch from 10^6 to 10^7. The count on the Display should perform as it did in Step 5 above, however, a full count interval should now register '080'.

2.2.7 Holding the SELF TEST switch at its INSERT ERRORS position, change the COUNT INTERVAL (BITS) switch from 10^7 to 10^8. The count on the Display should perform as it did in Steps 5 and 6 above, however, a full count interval should now register '800'.

2.2.8 Holding the SELF TEST switch at its INSERT ERRORS position, change the COUNT INTERVAL (BITS) switch from 10^8 to 10^9. The count will stop after approximately 11 minutes and 21 seconds. The Display should cycle through a complete count of 0 to 1000, a total of eight times. Since the Display contains only three digits, a count of 1000 will register as '000' with an OVERFLOW indication. The OVERFLOW indicator should come on at the first count of 1000. It will remain on after this point through the remaining seven cycles of 0 to 1000.

2.2.9 Holding the SELF TEST switch at its INSERT ERRORS position, change the COUNT INTERVAL (BITS) switch from 10^9 to CONT position and momentarily operate the RESET/RESYNC switch. The count on the Display should accumulate as in the preceding steps, and the OVERFLOW indicator should come on as the Display goes from '998' to '000' and stay on. Check that count continues for at least 12 minutes after OVERFLOW indicator comes on.

2.2.10 While holding the SELF TEST switch at its INSERT ERRORS position, momentarily operate the RESET/RESYNC switch. As it is operated the Display should clear to '000', and the OVERFLOW and COUNT indicators should go off; the COUNT indicator should come on again within 2/3 second of switch release.

2.2.11 Release the SELF TEST switch and return the COUNT INTERVAL (BITS) switch to its 10^6 position.

2.2.12 Set the MODE switch at ERRORS and momentarily operate the RESET/RESYNC switch. The Display indication should be '000' and all RECEIVE STATUS indicators should be off.

2.2.13 Push and hold the SELF TEST switch to INTERRUPT DATA. The NO DATA indicator should come on. The NO SYNC indicator will either come on and stay on, or blink rapidly and remain off. The LOST SYNC indicator may or may not come on; however, if the NO SYNC indicator is off, the LOST SYNC indicator must be on.

2.2.14 Release the SELF TEST switch. The NO DATA indicator should go off. The NO SYNC indicator should come on or remain on. The LOST SYNC indicator may be either on or off. The Display should show '888' with an OVERFLOW indication during the count interval, and any number with OVERFLOW at the end of the count interval.

2.2.15 Momentarily operate the RESET/RESYNC switch. The NO DATA, NO SYNC, and LOST SYNC indicators should remain off, and the Display should register '000' without OVERFLOW.

2.2.16 Set the SYNC MODE switch to AUTO, and hold the SELF TEST switch to INTERRUPT DATA. The NO DATA indicator should come on. The NO SYNC indicator will come on and stay on. The LOST SYNC indicator may or may not come on.

2.2.17 Release the SELF TEST switch. The NO DATA and NO SYNC indicators should go off. The LOST SYNC indicator should come on, if not already on. The display should read '000'.

2.2.18 Momentarily operate the RESET/RESYNC switch. The LOST SYNC indicator should go off.

2.2.19 Push and hold the SELF TEST switch at INSERT ERRORS. The Display should change by increments of two to a final count of '008'.

2.2.20 Holding the SELF TEST switch at its INSERT ERRORS position, change the COUNT INTERVAL (BITS) switch from 10^6 to 10^7 and place the ERROR BLOCK switch at its IN position. The Display should count by increments of one to a count of '040', which is one-half of the error count in step 6.

2.2.21 Holding the SELF TEST switch at its INSERT ERRORS position leave the ERROR BLOCK switch set at its IN position and change the MODE switch to its VIOLATIONS position. The Display should count by increments of one to a final count of '040'.

2.2.22 Determination of the operational readiness of the Test Set when operating in the APS TEST mode requires the use of an external bipolar signal source and bipolar violations detector. The Bowmar Model 271A (KS-20775, L1), 271B or 271C (KS-20775, L2) Error Rate Test Set may be used to fulfill this requirement. A Bowmar Model 271A will be used for the purpose of outlining a general test procedure.

Using patch cords with WE 310-type plugs at each end, connect a DS1 OUTPUT of the 271A to the DS1 INPUT of the instrument under test; connect any DS1 OUTPUT of the instrument under test to the DS1 INPUT ow the 271A. Set the MODE switch of the 271A to VIOLATIONS and the MODE switch of the instrument under test to APS TEST.

The table below lists all possible combinations of the APS TEST SEQUENCE and RANGE switches. Each combination is followed by a switch setting and display response which pertains to the testing instrument (271A). Complete each step of the table, observing that each result complies with table's requirement.

INSTRUMENT UNDER TEST			TESTING INSTRUMENT (271A)			
	APS TEST Settings		COUNT	Display		
Step	SEQUENCE Switch	RANGE Switch	INTERVAL (BITS) Sw.	Min.	Nom.	Max.
1.	START	x 10^{-4}	Any	0	0	0
2.	NOTR	x 10^{-4}	10^6	50	52	55
3.	TR	x 10^{-4}	10^6	200*	210*	220*
4.	NORST	x 10^{-4}	10^6	50	52	55
5.	RST	x 10^{-4}	10^7	30	33	36
6.	START	x 10^{-6}	Any	0	0	0
7.	NOTR	x 10^{-6}	10^8	30	33	36
8.	TR	x 10^{-6}	10^7	12	13	14
9.	NORST	x 10^{-6}	10^8	30	33	36
10.	RST	x 10^{-6}	10^8	1	2	3

* A test instrument with a 3-digit display is required to measure this error rate. The 271B or 271C (KS-20775, L2) is equipped with a 3-digit display.

3.0 OPERATION AND APPLICATIONS

3.1 Controls, Indicators, and Connectors

3.1.1 DS1 INPUT: a jack which accepts a WE 310-type plug; passes data from the system under test to the Test Set's Receiver.

3.1.2 DS1 OUTPUT: four jacks which accept WE 310-type plugs; serve as mutually independent outputs; each passes the Transmitter output to a system under test; each exhibits output impedance of 100Ω, ± 5%.

3.1.3 AUXILIARY OUTPUTS: four pin jacks and a BNC connector which monitor the signals listed below; one additional pin jack (GND) is provided for a ground connection.

(a) TRANSMITTER BIT SYNC: a 1.544 MHZ clock singal; square wave.

(b) TRANSMITTER WORD SYNC: a pulse, 340 nsec long, generated once per full cycle of the Transmitter sequence generator; changes this output's level from high to ground only for its duration.

(c) RECEIVER BIT SYNC: the clock signal as taken from incoming data by the Receiver clock extractor circuit.

(d) RECEIVER WORD SYNC: a pulse, 340 nsec long, generated once per full cycle of the Receiver sequence generator; changes this output's level from high to ground only for its duration.

(e) ERRORS: a pulse, 340 nsec long, for every error detected by the Receiver, changes this output's level from high to ground only for its duration.

3.1.4 MODE switch: a 3-position toggle switch used as follows.

(a) VIOLATIONS (up position) or ERRORS (down position): sets the Test Set for bipolar violations or logical errors; the Transmitter is set for the type of errors it must insert in the quasi-random test sequence, and the Receiver is set for the type of errors it must detect and count.

(b) APS (center position): connects the output of the Receiver section to the input of the Transmitter section; violations are inserted into the Receiver data pattern at a rate selected by the APS TEST RANGE and SEQUENCE switches.

3.1.5 ERROR BLOCK switch: a 2-position toggle switch used as follows.

(a) IN (up position): In this position, after an error is detected and displayed, additional errors are not counted during the 0.3 ms time period following that error.

(b) OUT (down position): In this position all errors are detected and displayed.

3.1.6 SYNC MODE switch: a 2-position toggle switch used as follows.

(a) AUTO (up position): sets the Test Set for automatic resynchronization in the event that synchronization is lost.

(b) MANUAL (down position): synchronization may be regained by operating the RESET/RESYNC switch.

3.1.7 SELF TEST switch: a 3-position momentary toggle switch used as follows:

(a) NORMAL (center position): for normal operation of the Test Set. With no connection to the DS1 INPUT (Receiver), the Receiver and Transmitter are directly linked. At the same time if the MODE switch is set for ERRORS, all indicators will be off and the Display will show no count; if the MODE switch is set for VIOLATIONS, the NO SYNC and LOST SYNC indicators will be held on while the NO DATA will be off, and the Display will show no count.

(b) INTERRUPT DATA (momentary up position): opens the link between Receiver and Transmitter, causing both the NO DATA and NO SYNC indicators to come on. Return to NORMAL position forces the NO DATA indicator off. If the SYNC MODE switch is at AUTO, the LOST SYNC indicator will replace the NO SYNC upon return to NORMAL. This function is disabled when a plug is inserted into the DS1 INPUT jack.

(c) INSERT ERRORS (momentary down position): inserts either logical errors or bipolar violations (depending on the MODE switch setting) into the Transmitter test sequence. These errors appear at the DS1 OUTPUT (Transmitter) jacks and are directed to the Receiver input via internal loop back wiring. In the Receiver, these errors exercise detection and counter circuitry and are registered on the Display. Since a known quantity of errors is injected into the Receiver, this process provides a quick self-test.

Note: The SELF TEST switch has no control over the Test Set when the MODE switch is set to the APS position. An externally connected bipolar signal source and violation detector are required to determine proper operation. (Reference par. 2.2.22.)

3.1.8 COUNT INTERVAL (BITS) switch: a 5-position switch whose settings determine the period of time, in bits, that the counter circuits will count errors: 10^6, 10^7, 10^8, 10^9, and CONT (for continuous tally).

3.1.9 DISPLAY INTERVAL (SEC) control: a variable potentiometer which determines the period of time the display will hold any given count; covers a range of from 1 to 10 seconds or continuous (HOLD).

3.1.10 APS TEST switches: a 5-position rotary switch (SEQUENCE) and a 2-position toggle switch (RANGE) control the insertion of bipolar violations when operating in the APS mode. Single violations uniformly spaced in time are inserted at the error rates listed in the table below.

APS TEST Switch Positions		Nominal Error Rate		
		Rate	Errors Per Sec.	BIT ERROR RATE
SEQUENCE	RANGE			
START	x 10^{-4}	0	0	
NO TR	x 10^{-4}	5 x 10^{-5}	77.22	20,000
TR	x 10^{-4}	2 x 10^{-4}	308.8	5,000
NO RST	x 10^{-4}	5 x 10^{-5}	77.22	20,000
RST	x 10^{-4}	$10^{-5.5}$	4.88	316,227
START	x 10^{-6}	0	0	
NO TR	x 10^{-6}	$10^{-6.5}$	0.488	3,162,279
TR	x 10^{-6}	$10^{-5.9}$	1.944	794,328
NO RST	x 10^{-6}	$10^{-6.5}$	0.488	3,162,279
RST	x 10^{-6}	$10^{-7.7}$	0.0308	50,118,690

3.1.11 RESET/RESYNC switch: a free-return toggle switch that resets the counter, initiates a new count, and resets the LOST SYNC indicator in the ERRORS mode, it initiates resynchronization and sets up a check of sync recognition circuits.

3.1.12 POWER switch: a 2-position toggle switch which controls application of power to the Test Set: ON (up position), OFF (down position).

3.1.13 RECEIVE STATUS indicators: four solid state indicators for the following purposes.

(a) NO DATA: is energized when data is not being presented to the Receiver (Refer to Section 4.3.5).

(b) NO SYNC: is energized when the Receiver is not synchronized to incoming data, or when the Test Set is in the VIOLATIONS mode.

(c) LOST SYNC: is energized when Receiver synchronization with incoming data has been lost and subsequently recovered; goes on when synchronization is recovered and remains on until the RESET/RESYNC switch is actuated. If the Test Set is in VIOLATIONS mode, LOST SYNC will be held on.

(d) ALL 1'S: is energized when the Receiver data is composed of continuous pulses. (Refer to Section 4.3.7).

3.1.14 Display: a 3-digit solid state indicator which presents a numerical readout of error count accumulated during any count interval.

3.1.15 OVERFLOW indicator: a solid state indicator which is energized when the error count exceeds the numerical capacity of the Display.

3.1.16 COUNT indicator: a solid state indicator which is energized during count intervals.

3.1.17 115 VAC 50-60 HZ power input: a recessed male connector; mates with one end of the Test Set's power cord.

3.1.18 3AG 1/2A SLO BLO fuseholders: two fuseholders used as follows.

(a) FUSE: holds the active power fuse.

(b) SPARE: holds a spare fuse.

3.2 Applications

The Error Rate Test Set can be used to test any digital transmission system or system component accepting a DS1, T1-type, bipolar signal and returning a similar signal. While the Receiver of the Test Set is equivalent in application to Bipolar Violations (BPC) Detectors for testing T1 lines, its additional bit-by-bit error detection capability, using a long pseudorandom sequence, is intended to test those system components which remove bipolar violations and/or are capable of causing logical errors without causing violations. The Transmitter of the Test Set is equivalent to and interchangeable with the Western Electric J98710R T1 Quasi-Random Signal Source and may be used independently of the Receiver for end-to-end tests or as a portable source. While the Transmitter provides a 3-volt bipolar signal for

input at the cross-connect bay, the Receiver may operate at or up to 750 feet from the cross-connect bay or similar source, at the monitor jack, or at numerous points using a bridge adapter. The following gives specific applications of the Error Rate Test Set in testing T1 lines or circuits, T1 to T2 (M12) multiplexers, and modems.

3.2.1 The Error Rate Test Set may be used to test any T1 line using either its bipolar violations (BPV) or logical errors detection schemes. The only constraint on the choice of detection is that logical errors detection requires the use of the standard test sequence whereas bipolar violations detection may be applied to any signal. An example of the latter type of detection, using message/data as the signal, would be the in-service monitoring of a circuit without the necessity of removing it from service. Figures 3-1 (a) and (b) depict typical applications of the Error Rate Test Set for checking T1 lines in both loopback and end-to-end configurations.

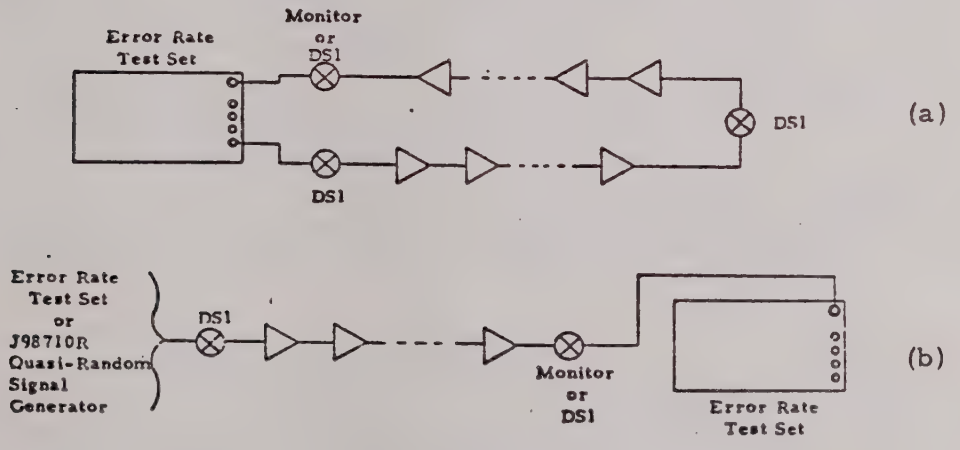


Figure 3-1: Loopback and End-to-End Applications

Traditionally, the Bell System J98710F Fault Locating Set (10F) has been used as a signal source when checking T1 lines, particularly during the acceptance testing that follows final construction, rerouting, or major repairs. If a line contains a splicing error, known as a double split, or if it contains other equally serious

problems, the line will pass all checks using a 10F but it will not support a terminal. The Error Rate Test Set will show such a line to be faulty because its quasi-random pattern stresses the line more realistically. It is therefore recommended that checkout with an Error Rate Test Set be added to Local Practices for line testing.

3.2.2 In some instances, idle circuits in an office may carry the standard test pattern merely to provide signal excitation. The Error Rate Test Set, used as a signal source, may be instructed to insert a fixed rate of either logical errors or bipolar violations into the test pattern sequence at a rate of approximately 8×10^{-6} in order to verify circuit identification. Added to the actual errors, such an increase can be recognized on most circuits.

3.2.3 Multiplexers and modems interfacing DS1, T1-type, signals to either higher order digital systems or analog systems are capable of removing bipolar violations from their inputs and/or can cause logical errors without violations appearing in the output data. It follows that the same is true of systems such as intercity spans, if they contain these components anywhere between their end points. The pseudo-random sequence and logical errors detection make it possible to evaluate such systems. It should be noted that BPV testing is not adequate for such systems as only the near-end bipolar equipment will be tested by BPV techniques. As an example, consider the DS1 to DS2, T1 to T2 (M12) multiplexer which combines four DS1 data streams into one DS2 stream. While the test sequence is needed only for the channel under check, the Error Rate Test Set provides four identical outputs to identically stress all four channels of the multiplexer. Not only are loopback and end-to-end tests possible, but tests over the higher order system or analog medium are also possible, as depicted in Figures 3-2 (a) and (b).

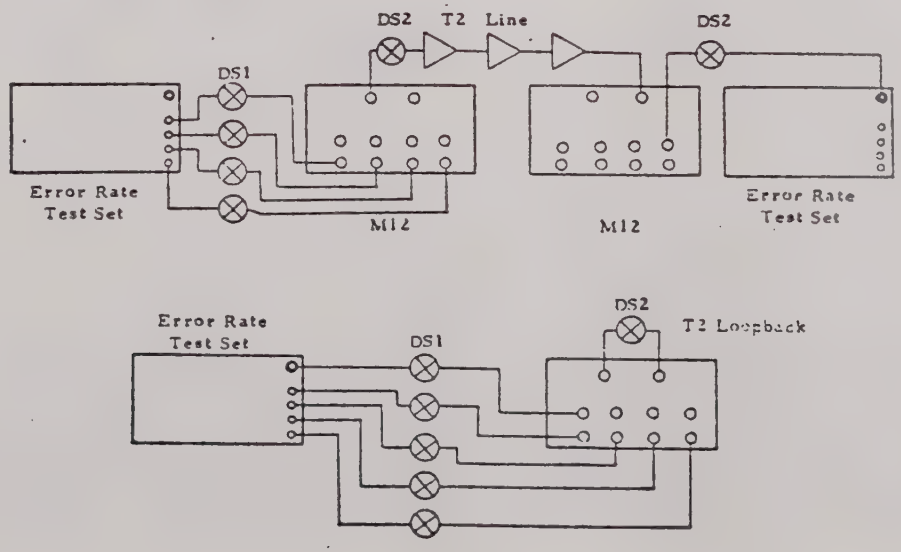


Figure 3-2: Higher Order System and Analog Medium Applications

CHAPTER 4

DESCRIPTION OF FUNCTIONS

4.1 General

Refer to the Block Diagrams (Figures 4-1 and 4-2 and the schematics of Section 6 to correlate descriptions offered in this section.

4.1. 1 Transmitter

The transmitter section of the Error Rate Test Set is a DS 1 (T1) type test source, arranged in two formats. One format consists of a continuously repeating Quasi-Random sequence of data bits identical to that provided by the Bell System test source (Western Electric J98710R T 1 Quasi-Random Signal Source). This sequence is derived from a 1,048,575 bit Sequence Generator which is self starting, and it is limited to fourteen consecutive zeros even though the sequence generator produces longer strings of zeros at several intervals. The second format is a retransmission of the data present at the test set's DS 1 input with all bipolar violations removed.

The transmitter output is a 1.544 mbps, 3 volt, bipolar, return-to-zero signal with training edge overshoot, available at four independent front level jacks.

For purposes of self-test and the test of other systems, the error rate test set can be made to insert errors into the transmitters output. A front panel switch offers a choice between either logical errors or bipolar violations.

The method used to insert errors depends on the selection of the transmitters source format. With the Quasi-Random source logical errors and bipolar violations are determined by the pattern contact of the sequence generator. When operating with the repeater format, bipolar violations insertion is controlled by a separate time base generator.

The Quasi-Random sequence generator produces four patterns of seventeen or more consecutive zeros each cycle. A pair of errors is inserted each time one of these patterns is detected, thereby producing a fixed error rate of eight errors per cycle, (1,048,575 bits).

Logical error insertions of a zero-to-one and a one-to zero conversion are performed by altering the function of the circuit which limits the output sequence to a maximum of fourteen consecutive zeros. This alteration is accomplished without violating either the fourteen-zero restraint or the bipolar format.

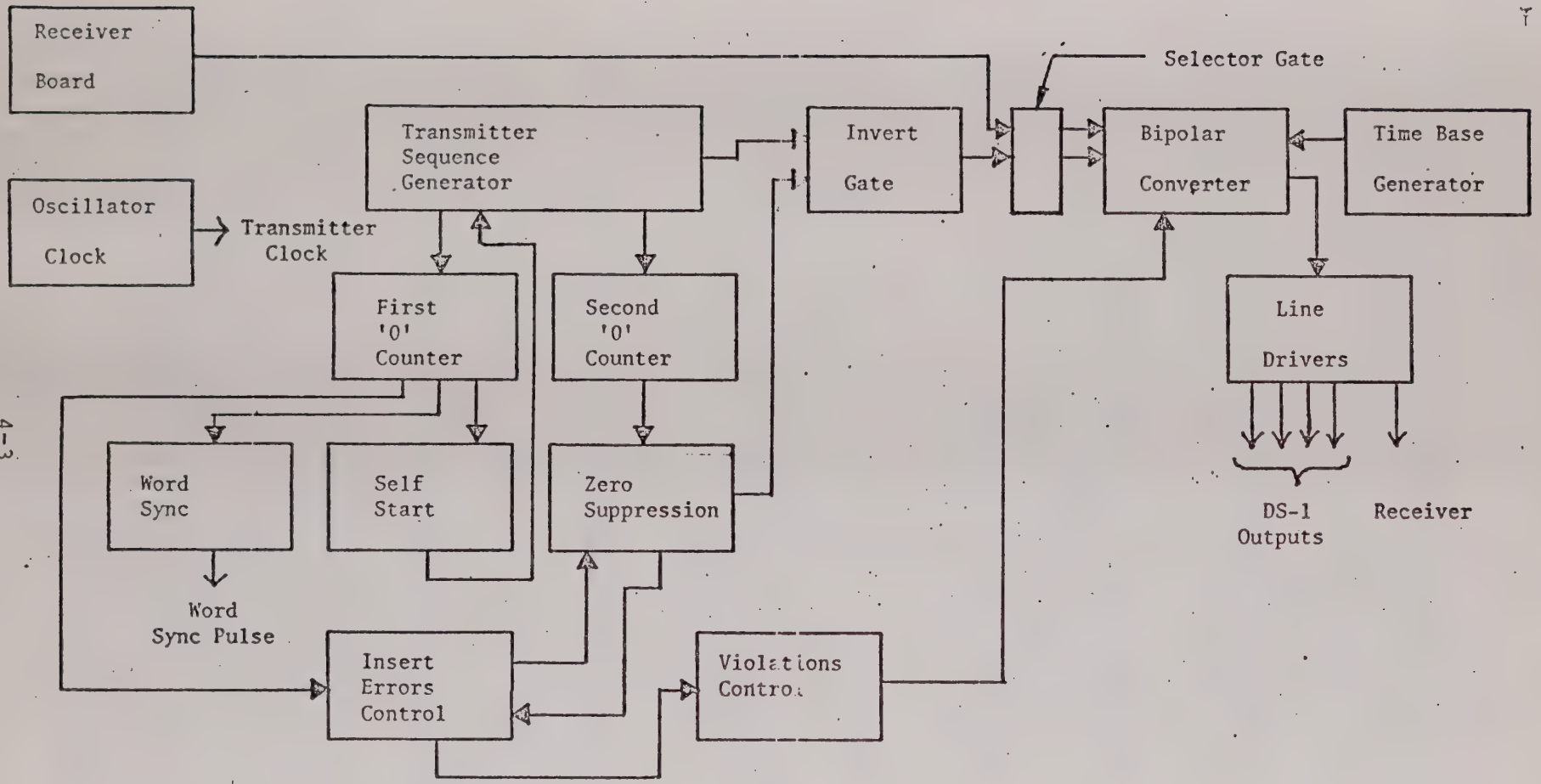
Bipolar violations consist of four consecutive ones, the first two of one polarity, and the second two of opposite polarity. This is accomplished by inhibiting the Bipolar Generator which normally alternates the polarity of each consecutive one, (whether or not they are interspersed with zeroes).

The first three, four, or five zeroes of the seventeen-or-more zero-condition-for-errors are thus forced to ones.

The chart below illustrates a typical condition of seventeen or more zeroes in the Sequence Generator. The Transmitter normally suppresses all zeroes in excess of fourteen by means of circuitry at the output of the Sequence Generator. However, when error insertion is desired, the normal functions of these added circuits is altered to inject the errors as shown.

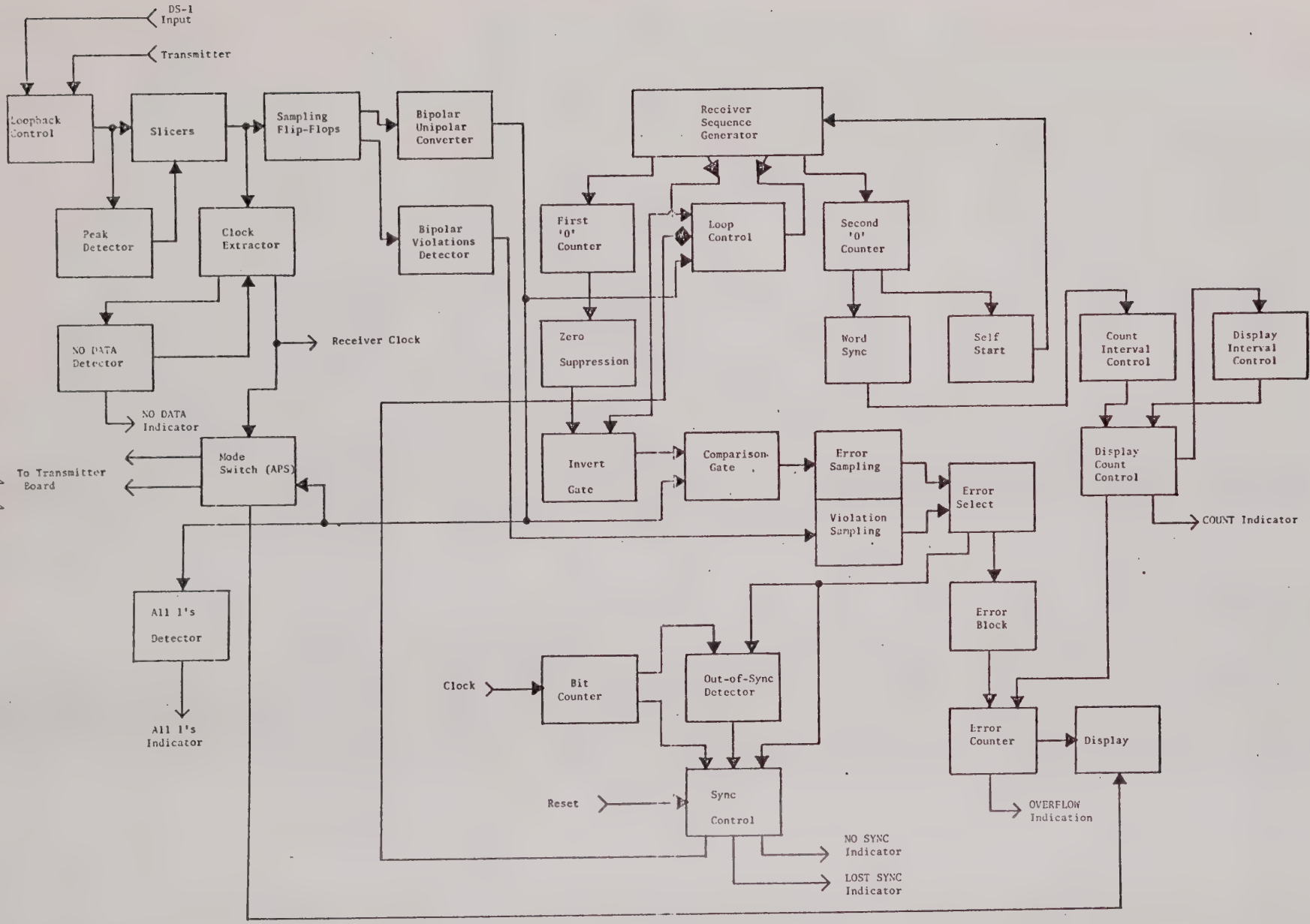
Description	Data Stream Segment
Any condition of 17 or more zeroes (18 shown) in Sig. Gen. output:	1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1
Corrected output (without errors):	1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1
Corresponding Xmitter Output, Bipolar Format:	+ - + - + 0 0 0 0 0 0 0 0 0 0 0 0 0 0 -
Corrected Sig. Gen. output with Logical Errors:	0 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 1
Correspond Xmitter output, Bipolar Format:	0 + - + - + 0 0 0 0 0 0 0 0 0 0 0 0 0 0 -
Errors:	X X
Corrected Xmitter output with Bipolar Violations:	+ + - - + 0 0 0 0 0 0 0 0 0 0 0 0 0 0 -
Violations:	X X

The time base generator is controlled by two front panel switches which select prescribed error rates for testing the transfer and reset thresholds of automatic protection switches. Single bipolar violations are inserted equally spaced in time.



BLOCK DIAGRAM OF TRANSMITTER SECTION

Fig. 4-1



Block Diagram of Receiver Section
Figure 4 - 2

4.1. 2 Receiver

Evaluation of data from a system under test takes place in the Receiver section of the Error Rate Test Set. Incoming data, in its bipolar format, is first sliced about its half peak amplitude point and subsequently sampled at the center of the bit period. A Peak Detector provides automatic threshold control for the slicers.

Clock pulses for the Receiver are taken directly from the reshaped data by a Clock Extractor circuit. In the event that data is discontinued, a No-Data Detector linked to the Clock Extractor signals the No-Data indicator on the front panel and inhibits clock pulses to the following circuitry.

Reshaped and Sampled data is directed to the Bipolar Violations Detector. In normal bipolar data, each consecutive one is alternated in polarity, whether or not there are zeroes in between. When two consecutive ones have the same polarity, the second is considered an error, and bipolar format has been violated. The output of the Bipolar Violations Detector is then ANDED with the output of the Bipolar/data from the Sampling circuit to a unipolar format.

All 1's Detector monitors the unipolar data, for actuating an indicator when this condition is present.

If the front panel MODE switch is set at VIOLATIONS, the output from the Bipolar Violations Detector is forwarded through the error block circuits to Error Count circuits for subsequent display. The sequence generator of the receiver, described below, continues to cycle solely for the purpose of providing a time base for test length selection via the COUNT INTERVAL switch. When operating in this capacity, the sequence generator is self starting but is not allowed to attempt to synchronize to the received data stream.

If the front panel mode switch is set at APS. the display is reset to zero and unipolar data together with an output from the clock extractor are directed to the transmitter section.

If the front panel MODE switch is set at ERRORS, the count from the Bipolar Violations Detector is ignored. Instead, the unipolar data stream is routed to the Receiver Sequence Generator. This generator differs from its transmitter counterpart only in its monitor points, and in a modified feedback loop. Otherwise, it is capable of the same 1,048,575 bit test pattern.

The key difference between Transmitter and Receiver Sequence Generators is the latter's modified feedback loop. This loop is arranged to be opened or closed. In its closed mode, the Receiver generator behaves exactly like the Transmitter generator; it is a self-starting generator for the 1,048,575 bit test sequence. In its open mode, however, it is injected with the received test pattern in unipolar format. If the received test pattern is without error, it will deceive the generator into behaving as a closed loop device, thus synchronizing the generator to the received pattern.

The self-synchronizing feature of the Receiver Sequence Generator may be initiated automatically or manually, depending on the setting of the SYNC MODE switch (two settings: AUTO or MANUAL) on the front panel. In the MANUAL mode, loss of sync is indicated by the NO SYNC indicator; resynchronization may be gained by pressing the RESET/RESYNC button.

Once Sequence Generator sync is achieved and the loop is again closed, received data is compared with the Generator output for logical errors. Error Counter for subsequent display. As with violations, the Display will show errors per cycle of the test sequence, or per ten or one hundred cycles depending on the setting of the COUNT INTERVAL switch. The exception to errors per cycle (s), for both logical errors and bipolar violations, will be a cumulative tally made when the COUNT INTERVAL switch is at its "CONT" setting.

4.2 Transmitter Circuits

When selected, the block error circuit inhibits the count of errors for a period of .3 hours after a count has been added to the error counter.

4.2. 1 1.544 MHz Clock (A10)

A 3.088 MHz crystal oscillator is divided by a single JK flip-flop to provide a 1.544 MHz symmetrical, two-phase clock. Transistors Q1 and Q2 make up the oscillator, with Q3 and Q4 serving as an emitter-follower and a buffer. Q1 and Q2 are connected as a two-transistor amplifier with negative feedback. Q1 provides most of the gain. Negative feedback stabilizes the bias points and holds crystal current to a good operating range. Positive feedback through the crystal is sufficient to produce oscillation. Oscillation occurs at the frequency of minimum crystal impedance, the series-resonant frequency. The oscillator output is divided by IC17A. Resultant clock pulses are distributed throughout the Transmitter to control all timing functions.

4.2.2 Transmitter Sequence Generator (A10)

Quasi-random test patterns, or sequences, issued by the Transmitter are derived from a 20-stage shift-register generator whose feedback is taken from stages 17 and 20. The Generator is contained by I.C.'s 1A through 4B, with feedback directed through the exclusive-or circuit of IC8B.

The Generator provides a continuously repeating sequence of 1's and 0's. Each sequence is made up of all but one of the 220 possible combinations of 20-bit states, for a total of 1,048,575 bits. The one exception is the all-zero state in which the Generator will not function. When the all-zero state does occur, it is eliminated by a Self Start circuit (see Section 4.2.4). Each resultant sequence therefore contains strings of 1's up to and including 20 bits and strings of 0's up to and including 19 bits.

The main output of the Generator is taken from the 20th stage. Additional outputs are taken from the 2nd, 5th, 6th, and 7th stages. These auxiliary outputs enable sequence bits to be monitored during their serial progression through the chain of register stages. The bits shift a stage at a time with each Clock pulse.

The sequence monitored at the auxiliary outputs is the same as that issued at the main output. However, where each auxiliary output is some number of stages ahead of the main output, the sequence at each auxiliary output is the same number of bit periods ahead in time of the sequence at the main output. This feature allows a "preview" of the output for purposes of possible correction or alteration in subsequent circuits. Specific purposes of the auxiliary outputs are described in the sections that follow.

4.2.3 Transmitter '0' Counters (A10)

Two separate counters are connected to auxiliary outputs of the Sequence Generator to register any series of successive 0's. Both counters are actually incremented by Clock pulses, but each is reset by registration of a '1' so that effectively they are counting 0's.

The first counter is a 5-bit binary counter connected to the 2nd-stage output of the Sequence Generator. It is used to aid the Self Start circuit (see Section 4.2.4), to provide a sync pulse at the beginning of the test sequence, and to control the injection of errors. Its components are IC's 13A, 5A, and 7A.

The second counter is a 4-stage counter contained by IC6A. It is connected to the 5th-stage output of the Sequence Generator and at this tap it is 3 bits behind the 2nd-stage tap. This counter signals the Zero Suppression Control (see section 4.2.7) when it has registered fifteen consecutive 0's in the test sequence. Thus, the number of 0's delivered to the line or device under test may be limited. This limitation is imposed without disturbing the contents of the shift register.

4.2.4 Transmitter Self Start Circuit (A10)

Self starting is initiated by a single gate, IC10A, which is activated by a count of 24 from the First '0' Counter (see Section 4.2.3). This count is possible only if the Sequence Generator is in the all-zero state.

As described in Section 4.2.2, all-zeroes in the Sequence Generator is an illegal state in which the Generator cannot function. Upon registration by the First '0' Counter of 24 0's, the Self-Start circuit is activated to force a single 1 into the Sequence Generator. Appearance of the 1 cancels the illegal state and stimulates the Generator into normal operation.

4.2.5 Transmitter Word Sync Circuit (A10)

The Word Sync Circuit consists of a single gate, IC9B, used in conjunction with an inverter, IC13D. It is connected to the First '0' Counter to respond to the passage of 19 0's followed by a 1 through the Sequence Generator. Since this condition occurs only once every 1, 048,575 bits, it is used to mark each full cycle of the Sequence Generator. The Word Sync Circuit responds to this count by providing a sync pulse to a front panel test point.

4.2.6 Insert-Errors Control (A10)

Error injection into the test sequence is initiated by holding the SELF TEST switch at its INSERT ERRORS position. Errors may be logical or they may be bipolar violations, depending on the MODE switch setting (the MODE switch offers two settings: VIOLATIONS or ERRORS).

Errors are forced into the test sequence after its issue by the Sequence Generator. Insertion is triggered by the First '0' Counter's detection of seventeen or more consecutive 0's, counted as they pass through the Sequence Generator. This condition occurs four times during each cycle of the test sequence. In each instance, a pair of errors, rather than a single error, is inserted so that both a 1-to-0 and a 0-to-1 conversion is accounted for. Thus for each cycle of the test sequence, four pairs of errors may be injected.

Insert-Errors Control circuitry is made up of several gates, inverters, and a single flip-flop. These are IC's 9A, 13C and E, 14D, 15A, 18A through C, and 19A through C. IC15A is the lone flip-flop. The count of seventeen 0's is detected by IC9A and used to set the flip-flop. The remaining gates then act as steering circuits enabling the Insert-Errors Control to interact with either the Zero Suppression Control or the Violations Control (Sections 4.2.7 and 4.2.8 respectively) in the forcing of errors.

4.2.7 Zero Suppression Control (A10)

The Second '0' Counter being a 4-stage device, as described in Section 4.2.3, it can count up to fifteen 0's. The test sequence, as furnished at the Test Set output, is intended to contain no more than fourteen consecutive 0's. Therefore, when the Second '0' Counter registers its fifteenth consecutive 0, it activates the Zero Suppression Control to convert all excess 0's at the Sequence Generator's output to 1's.

The Zero Suppression Control is made up of gates, inverters and a flip-flop. These are IC's 10B, 11A through D, 14A through C, and 15B. The flip-flop is IC15B.

The second '0' Counter taps the 5th stage of the Sequence Generator. Its count is therefore fifteen bits ahead of the Generator's output at the 20th stage. By the time the Counter records the fifteenth 0 of a string, the first 0 of the same string is at the Generator's output. At the same time, the gate of IC10B detects the count of 15 and signals the Zero Suppression Control into action. The Zero Suppression Control responds by converting the first and subsequent 0's of the string to 1's. Zero-to-one conversion continues until a 1 is detected at the 6th stage tap of the Sequence Generator. The appearance of a 1 at the 6th stage tap turns off the Zero Suppression Control, and the last fourteen 0's of the string are allowed to pass.

Operation of the Zero Suppression Control is modified slightly when logical errors are to be inserted. As discussed in Section 4.2.6, errors are inserted when the Sequence Generator contains seventeen 0's. However, a signal from the Insert-Errors control and the First '0' Counter turns on the Zero Suppression Control one bit earlier than normal. In this way, the bit preceding the string of 0's at the Sequence Generator output is converted to a 0, thus providing an error of the 1 to conversion type. In addition, steering gates in the Insert-Errors Control switch the Zero Suppression Control turnoff from the 6th stage to the 7th stage of the Sequence Generator, thus turning off the Zero Suppression one bit later than normal and forcing an extra zero-to-one conversion. This conversion is also an error. The net result for the seventeen 0 string is therefore two errors, a 1 to 0 and a 0 to 1 conversion.

The following chart provides a visual representation of Sequence Generator contents and output, with and without error pairs.

```
Sequence
 Generator        1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Normal
 Output           1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0

Output With
 Logical          0 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0
 Errors         #1      #2
                Error   Error

                          Time
```

4.2.8 Bipolar Violations Control (Violations Mode) (A10)
The Bipolar Violations Control, consisting of IC's 21A and 12B, acts upon instructions from the Insert-Errors Control to inject violations into the Test sequence data stream. This is accomplished by disabling the Bipolar Generator (Section 4.2.11) for the appropriate bits of the data stream.

IC's 21A and 12B make up a 3-bit binary counter and a sampling flip-flop, the latter for timing adjustment purposes. When violations are to be inserted, per actuation of the SELF TEST and MODE Switches, the 3-bit counter commences to register Clock pulses. The output of the counter's first stage is then connected to inhibit the Bipolar Generator, which is presented a string of forced '1's' during this process. The Bipolar Generator is inhibited after the counter's first 1, enabled after the second, and inhibited again after the third. When the counter registers a count of 4, the Insert-Errors Control and Bipolar Violations Control are both reset.

During each 4-bit operating period, the Bipolar Violations Control causes two consecutive 1's of one polarity followed by two consecutive 1's of the opposite polarity. These constitute an error-pair. As discussed in Section 4.2.6, there are four error-pairs per test sequence. Bipolar Violations are inserted without causing logical errors.

4.2.9 Invert Data Gate (A10)
IC8A is an Exclusive OR gate through which the Zero Suppression Control inverts output bits of the Sequence Generator. The inversion forces each 1 to a 0 and each 0 to a 1.

4.2.10 Selector Gate (A10)
The Selector gate, IC22A through D, routes either the output from the invert data gate or sampled receive data to flip-flop IC12A. The invert data gate is selected when the Mode Switch is set to either its' violation or error position. Receive Data is selected in the APS position.

The output of IC22D is sampled and delayed one-half bit by IC12A. This delay eliminates transients which result from simultaneous switching of the many circuits controlled by Clock pulses. The output of the sampling flip-flop is then "ANDED" with Clock pulses through IC16A to obtain a return-to-zero data format for the Bipolar Generator (Section 4.2.11).

4.2.11 Bipolar Generator (A10)

A single flip-flop, IC7B, and four gates, IC's 16C and D and IC8C and D make up the Bipolar Generator. Its function is to alternate the polarity of all 1's in the test sequence regardless of the interspersion of 0's. Thus, when a 1 is generated with one polarity, the next 1 will have the opposite polarity whether or not there are 0's between the two 1's.

Bipolarization is triggered by the trailing edge of each 1 in the data stream. At this instant, the flip-flop of IC7B toggles so that the next 1 is transmitted with the opposite polarity. Two gates, IC8C and D, delay the toggle input to the flip-flop slightly to insure a correct time relationship with the inhibit input from the Bipolar Violations Control circuit.

The output of the Selector Gate is "ANDED" with each of the toggle flip-flop outputs to provide necessary steering for the Line Drivers (Section 4.2.14). When the test set is operating in the Violations Mode, violations are added by inhibiting the toggle of flip-flop IC7B (Bipolar Violations Control, Violations Mode, Section 4.2.12). Violations are added in the APS Mode by inverting the output of IC7B when commanded to do so by the Bipolar Violations Control (APS Mode).

4.2.12 Bipolar Violations Control (APS Mode) (A10)

The Bipolar Violations Control circuitry consists of IC24 A and B, and IC23 A and B. The function of this circuit is to inject violations into the Received Data Stream. This task is accomplished by inverting the output of the Bipolar generator (Section 4.2.11) when stimulated by a clock output from the Time Base Generator (Section 4.2.13).

Flip-Flop IC24B is toggled by the output of the Time Base Generator forming a symmetrical clock at a frequency of one half the generators output. This clock is applied to IC24A which samples and retimes it to the transmitter 1.544 MHz clock. Exclusive or gates IC33A and B invert the output of the Bipolar Generator IC7B when the output of IC24A is at a logical one. This results in a violation for each transition of flip-flops output. The symmetrical nature of this output produces violations equally spaced in time at a rate determined by the Time Base Generator.

4.2.13 Time Base Generator (A11)

The Time Base Generator, consisting of IC's 1 through 8 and IC16, determines the rate at which Bipolar Violations are inserted when the test set is operating in the APS Mode. The approach is to selectively divide the output frequency of a free running oscillator. The oscillator operates at a frequency of 308.1 Hz and is built around IC1. Two tandem connected counters IC's 2 and 3 perform a divide by one hundred and sixty function. Steering logic, IC4, A through D, selects either the oscillator output or the oscillator output divided by one hundred and sixty from IC3. The selection is controlled by the front Panel APS test range switch.

A second selector gate is provided by IC7 A through C and IC8B. This selector can choose between the output of the first selector gate (IC4D), the output of the IC4D divided by four, or this output divided by 64. The binary counters IC5 and 6 are connected to provide the divide by four and sixty-four function. The output of the second selector gate IC7C is the output of the Time Base Generator. This output is inhibited when operating in a mode other than APS by application of a '1' to IC8A. Inverters IC16A through C provide an interface between the APS test sequence switch and this selector gate. The sequence and range switches work together to determine the output frequency on the time base generation.

4.2.14 Line Drivers (A10)

Each of the Bipolar Generator's two outputs is directed to a paralleled pair of driver transistor switches (Q5-Q8) whose outputs are tied to an outer tap of a center-tapped transformer primary. The paralleled transistor switch arrangement ensures a higher speed of operation and higher current capacity. One switch pair with half the primary handles positive bits of the bipolar signal while the other pair and half handle the negative bits.

The Transformer is trifilar wound with two of its windings connected as the center-tapped primary. The third winding serves as the balanced output, padded as necessary and distributed to the front panel jacks and to the receiver.

Shaping of the inherently square signal bits into T1 pulse shape with trailing edge overshoot is accomplished with a passive RLC circuit. The RLC circuit is connected across the transformer primary.

4.2.15 Pads (A10)

The output of the Line Drivers is connected to a parallel arrangement of pads which serve to drop output voltage to three volts while providing a measure of isolation between outputs. Four pads link the line drivers to front panel jacks. A fifth pad of higher attenuation provides a loop back path from the Transmitter to the Receiver sections for self test purposes.

The output of each of the five pads is arranged to terminate in 100 ohms if it is not in use. This presents a constant impedance to the Line Drivers and pulse-shaping network, regardless of the number of outputs in use.

4.3 Receiver

4.3.1 Loop Back Control (A13)

A reed relay (K1) and its coil driver (Transistors Q1 and Q2) are used to open or close the bridge between Transmitter and Receiver. The bridge is closed unless a plug is inserted into the Receiver input jack, or unless the SELF TEST switch is held at its INTERRUPT DATA position. In its open position, the relay is de-energized.

4.3.2 Peak Detector (A13)

To accommodate bipolar inputs of widely varying amplitudes, a Peak Detector circuit supplies a threshold level to the Slicers (Section 4.3.3). This circuit is a full-wave type which effectively converts its bipolar inputs to unipolar. Its output is taken from a voltage divider which, coupled with capacitor (C3), supplies a level half the peak amplitude of each incoming '1' bit. Transistors Q3 and Q4 and divider resistors R10 and R11 make up the Detector.

NOTE: Transistors Q3, 4, 5, 6 and diode CR2 are contained in a single monolithic device (IC8). This single device was chosen over separate transistors to take advantage of the closely matched substrate.

4.3.3 Slicers (A13)

A pair of Slicer circuits compares the outputs from the two Transformer T1 secondary extremities to the output of the Peak Detector to establish a peak level for each incoming '1' bit. Bits of one polarity are handled by Transistor Q5 in conjunction with IC5A and B, while the opposite polarity uses Q6 and IC5D and C. A separate output for both polarities preserves the polarity information for the violation detector. The entire function is performed by a dual-high-speed line receiver which gives high speed operation with little offset error.

4.3.4 Clock Extractor (A13)

In order that the Receiver can properly synchronize with incoming signals it derives clock pulses from incoming data rather than an internal clock. The clock Extractor monitors and effectively rectifies both Slicer outputs through IC6A and Q7. The rectified signal is then converted into a series of pulses, one for each '1' bit, which are applied to a very high-Q-circuit. The result is a ringing output of more than adequate duration to supply clock pulses during strings of '0' bits of the maximum allowable length. Thus, a 1.544 MHz frequency component is extracted from the received signal regardless of '0' bits.

The output of the high-Q-circuit is phased as required and applied to a separate slicer for shaping. The output of the slicer is directed to IC7B together with the output of the No Data Detector. The output of IC7B is a symmetrical clock signal of proper phase for the entire receiver. This output is inhibited when No Data is detected to prevent the tally of errors due to this condition.

4.3.5 No Data Detector (A13)

The No Data Detector, consisting of IC9 monitors the output of the slicers through IC6A. The dual retriggerable monostable multivibrator IC9 is connected in a tandem arrangement, where the second stage is triggered by an output of the first. The first stage is continuously retriggered by data pulses from the output of IC6A. In the event that data is interrupted, retriggering is discontinued, permitting this stage to complete its monostable function. The time constant of the first stage (26.5 microseconds) is determined by circuit elements R57 and C26. This time constant corresponds to 41 ± 9 zeroes, which defines the No Data threshold. The second stage, when triggered by the No Data condition detected by the first stage, generates a pulse of 100 ± 20 ms. An output from this stage is applied to the gate input of the first stage which inhibits triggering of the first stage for a 100 ms period following detection of No Data. The 100 ms time constant is determined by components R56 and C27. The output of the No Data circuit is extracted from the first stage. This output is directed to both the No Data indicator buffer through IC6D and to the clock extractor circuit IC7B.

4.3.6 Bipolar/Unipolar Converter (A13)

Positive and negative data bits are carried by their own separate lines from their respective slicers to D-type sampling flip-flops. (IC's 1A and B). The flip-flop outputs are OR'ed by IC3A to be converted to a single, unipolar, NRZ (non-return-to-zero) signal.

4.3.7 All 1's Detector (A11)

The all 1's detector, consisting of IC16D, 15C + Q1, provides a visual indication to an operator when a sequence of continuous pulses is being received by the test set.

Transistor Q1 with components R14, R13 and C7 form a integrator which monitors the output of the unipolar detector (Section 4.3.6). Inverter IC16D functions as an interface between the unipolar detector and Q1. Buffer gate IC15C monitors the output of the integrator at capacitor C7 and drives a front panel indicator. The indicator is actuated when the voltage across C7 reaches the buffer's threshold voltage, indicating an all 1's condition.

4.3.8 Bipolar Violations Detector (A13)

This circuit consists of a pair of two-stage binary counters, IC's 2A and B for one and IC's 4A and B for the other. A gate for each counter AND's the Receiver Clock pulses with a slicer output to give return-to-zero signals which toggle and reset the counters.

When a '1' of positive polarity is received, the first stage of one counter is set while the other counter is cleared. When a '1' of negative polarity follows, the first counter is cleared while the second is set for a count of 1. Should two '1's of the same polarity arrive, one of the counters will register a count of 2 to indicate bipolar violation.

OR'ing the two counter outputs and AND'ing the result with the unipolar data stream completes the bipolar detection process. This arrangement enables detection of violations even though the consecutive 1's are separated by one or several 0's. It also allows registration of a string of bipolar violations. The resultant violations data is channelled to the Error Counters for subsequent display, provided the MODE switch is set for VIOLATIONS.

4.3.9 Receiver Sequence Generator (A12)

Should the MODE switch be set to ERRORS, incoming data as processed by the Bipolar/Unipolar Converter is directed to the Receiver Sequence Generator and associated circuits whose purpose is the detection of logical errors.

The Receiver Sequence Generator produces a test sequence identical to that of the Transmitter Generator. However, the Receiver Generator differs somewhat in configuration. First, its outputs are taken from different stages. Second, its timing is derived by extracting clock pulses from incoming data rather than an internal clock. Finally, its feedback loop may be opened to receive incoming data rather than its own output for the purpose of synchronization.

The intent of different output locations is explained in sections that follow, while clock-pulse extraction is accounted for in Section 4.3.4. This leaves, then, manipulation of the feedback loop.

With the feedback loop closed, the Receiver Generator behaves exactly as the Transmitter Generator in working up the 1,048,575 bit test sequence. But it is necessary to synchronize the test sequence from the Receiver Generator with that of an incoming signal if a bit-by-bit comparison of data bits is to be performed. This synchronization is achieved by opening the feedback loop and inserting the incoming signal in place of the Generator's output. The generator responds as if the loop were closed, and within a very brief time interval (20 data bits later) the Generator's output corresponds exactly with the data being inserted in its place.

Should incoming data contain error bits during synchronization, the process will be delayed. In order for synchronization to be achieved, incoming data must contain at least 20 error-free bits. An additional 40 error-free bits must be received in order to confirm resynchronization. And once synchronization is confirmed, the Generator's Sync Control circuit (Section 4.3.20) forces the feedback loop to its closed status so that normal operation may resume.

Should synchronization be lost during normal operation, the loss is detected by the Out-of-Sync Detector (Section 4.3.19). In the auto sync mode, this circuit then signals the Sync Control to re-open the feedback loop for re-synchronization. Resynchronization can also be initiated by depressing the RESET/RESYNC button.

Generator components are IC's 1A and B, 2A and B, 3A, and 4A. IC11B serves as the exclusive-or circuit in the feedback link. The Generator's output is taken from IC4A, which is stage 17. And the bridge between stages 17 and 18 contains the Loop Control circuitry (Section 4.3.10) which opens or closes the feedback loop.

4.3.10 Loop Control (A12)

The gate system, made up of IC's 8A, -B, and -C, effectively forms a SPDT switch which controls the Receiver Generator's feedback loop. The input to stage 18, from IC8B, is the common line. In one mode, stage 18 receives data directly from the output of stage 17, while in the other it receives the incoming, unipolar data signal. IC6E is an inverter through which the Sync Control (Section 4.3.20) may force the Loop Control to switch stage 18 to the incoming data line, should synchronization be required. If the Generator is properly synchronized to incoming data, there will be no signal from Sync Control; the Loop Control will therefore switch data from stage 17 to stage 18.

4.3.11 Receiver '0' Counters (A12)

Two '0' Counters are connected to the Receiver Sequence Generator. Their functions and operation are identical to those described for the Transmitter.

The first counter monitors the output of stage 1. It is a 4-bit binary counter used in limiting the number of consecutive 0's in the Receiver Generator's test sequence and is contained in IC5A.

The second counter is a 5-bit affair connected to the Generator's stage 19 output. It serves in the generation of a "word-sync-pulse" (Section 4.3.13), and to make the Generator self-starting for bipolar violations measurements. (For bipolar violations measurements, the Generator serves only in the making of a word-sync-pulse for each cycle of the test sequence).

4.3.12 Receiver Self-Start Circuit (A12)

Operation and function of this circuit are identical to its Transmitter equivalent. It differs in its interfacing, however, in that its input is taken from the Second '0' Counter, and its output is routed to the Generator's 19th stage. The IC8D gate is the entire circuit.

4.3.13 Receiver Word-Sync Circuit (A12)
The Word-Sync Circuit is also a duplicate of its Transmitter counterpart. Its input gate, IC7B, is connected to the Second '0' Counter, while its output is directed through inverter IC12D and Transistor Q10 (A13). The output is also routed to the Display/Count Control and the Count Interval Control. In the latter circuitry, the Word-Sync pulse serves as the major time base.

4.3.14 Receiver Zero-Suppression Circuit & Invert Data Gate (A12)
Input gate IC7A, of the Zero Suppression Circuit, is connected to monitor the First '0' Counter for a count of fifteen 0's. A second input is taken from the 3rd stage of the Sequence Generator to serve as a reset line for the Suppressor's flip-flop, IC10A.

As does its Transmitter namesake, the Zero Suppressor limits consecutive 0's from the Sequence Generator to a total of fourteen. While more than fourteen 0's may be generated, the first fifteen are registered by the First '0' Counter. Input gate IC7A responds to the count of fifteen by setting IC10A with a signal delivered through IC's 12B and C and 13A. At the same instant IC10A is set, the last 1 prior to the string of 0's is issued from the main output, stage 17, of the Sequence Generator.

When IC10A is set, all 0's issued from the Generator are converted to 1's by Invert Gate IC16A, while all 1's are maintained. Thus, the last 1 issued prior to the string of 0's is kept intact while all 0's that follow are converted to 1's. This process continues until appearance of a 1 at the Generator's 3rd stage output. A 1 at the 3rd stage output resets IC10A. The remaining 0's. one in each of the following Generator stages are allowed to pass. Since there are fourteen stages between stage 3 and the main output at stage 17, only fourteen 0's are actually issued without conversion. Thus, consecutive 0's from the Generator are limited to fourteen in all.

4.3.15 Invert Data & Comparison Gates (A12)
IC16A is merely a NAND gate used for an OR function. Since the Receiver required only 0-to-1 conversions, and not the 1-to-0 conversions used by the Transmitter, an Exclusive-OR gate is unnecessary. The output of the Invert Data Gate is not sampled, as in the Transmitter, but is passed directly to the Comparison Gate.

The Comparison Gate, IC11A, is an Exclusive-OR used to compare the received-data-stream, from the Bipolar/Uinpolar Converter, with the test pattern from the Sequence Generator. Comparison is performed bit-by-bit, and any differences appear as logical ones at the output of the Comparison Gate.

4.3.16 Sampling Flip-Flops (A12)
The output of the Comparison Gate and the output of the Bipolar Violations Detector are sampled by D-type flip-flops IC15A and IC15B respectively. Thus, detected logical errors and bipolar violations are simultaneously available to the Error-Select Circuit (see below). These error signals are provided in NRZ (non Return to Zero) format.

4.3.17 Error-Select Circuit (A12)
The outputs of both Sampling Flip-Flops connect to Error-Select Circuit gates IC13B and IC14B, where they are AND'ed with Clock pulses. By AND'ing the Sampled outputs with Clock pulses, their NRZ format is converted to RZ format, or a separate pulse for each error, by the Error-Select input gates.

Bipolar violations can be AND'ed with Clock pulses at the Error-Select input gate only when the Mode switch (front panel) is set to "Violations". Logical errors, however, are AND'ed with Clock pulses at the corresponding input gate whenever they appear. The resulting logical error pulses are inverted then directed to a second gate, IC13C. At this point they are also directed to the Out-of-Sync Detector and the Sync Control, which function normally regardless of the position of the mode switch. Passage of logical error pulses through the second gate, IC13, is then dependent on Mode switch setting. Thus, either the passage of bipolar violations through Error-Select gate IC14B or the passage of logical errors through Error-Select gate IC13C depends on the Mode switch setting.

From the selectable gates either error signal is OR'ed through IC13D to the gate IC14C. Passage through IC14C to Counter circuitry then depends on signals from the Display/Count Control.

4.3.18 Bit Counter (A12)
The Bit Counter is made up of IC's 22 and 23 with gate IC21A. This circuit provides a pulse every 20 bits to the section of Sync Control Circuitry that confirms synchronization. It also provides a narrow pulse every 40 bits to the Out-of-Sync Detector. The purposes of both pulse types will be explained under sections describing their respective destinations.

4.3.19 Out-of-Sync Detector (A12)
The Out-of-Sync Detector is essentially an error counter which separates incoming data into 40-bit blocks and checks each block for a quantity of errors in excess of twelve. More than twelve errors indicates an out-of-sync condition.

The detection process is accomplished by counting logical-error pulses from the Error-Select circuit during the 40-bit interval allowed by the reset pulse from the Bit Counter. Counting takes place in IC24A. The gate of IC19C opens for a count of 12 or more to release an out-of-sync pulse to the Sync Control Circuit.

4.3.20 Sync Control (A12)

Sync Control Circuitry performs the opening and closing of the Sequence Generator feedback loop, and it regulates operation of both the NO SYNC and LOST SYNC indicators on the front panel. Its primary components are IC's 18A and 18B which make up a 2-bit shift register for purposes of sync confirmation.

Both stages of the 2-bit register are set under any of the three following conditions:

1. Actuation of the RESET/RESYNC button on the front panel.
2. A pulse from the Out-of-Sync detector.
3. Detection of an error before the shift register can be cleared. The shift register has a logical zero input and is toggled by the 20-bit output of the Bit Counter. There must therefore be two consecutive error-free blocks of twenty bits before the register is cleared.

Four gates at the shift-register output control the NO SYNC indicator and status of the Sequence Generator loop. If the second stage of the shift register is set, the Receiver is out of sync and the NO SYNC indicator is energized. Also, with the MODE switch set to VIOLATIONS, the NO SYNC indicator is forced on regardless of sync status. One of the four gates controls the NO SYNC indicator, while the remaining three control status of the Loop Control circuit.

Of the three remaining gates, one allows the shift register to control status of the Sequence Generator's feedback loop only in the automatic sync mode, while another gate ORs the automatic sync control with the manual sync command from the RESET/RESYNC pushbutton. The final gate inhibits the Sequence Generator's feedback loop from being opened by any means when the test set is set to measure bipolar violations.

For Violation measurements the Sequence Generator is used as a time base only, and it need not be synchronized with the received data. This is achieved by the final gate and the self-start capability of the Generator.

Finally, one flip-flop and one gate control operation of the LOST SYNC indicator. The flip-flop is set by output of the gates, mentioned above, when sync has been regained, and it energized the indicator. The flip-flop can be reset only by operating the RESET/RESYNC switch. The gate forces the indicator on when the test set is instructed, via the MODE switch, to measure Violations.

4.3.21 Count Interval Control (A12)

The Count Interval Control consists of two decade counters, IC's 27A and 28A, along with several gates, and the COUNT INTERVAL switch (front panel). The counters tally word-sync

pulses and provide output at one, ten and one hundred word intervals. The appropriate output is selected via the COUNT INTERVAL switch position and selection gates, and it is provided to the Display/Count control circuit.

Since a word-sync pulse is generated once for each cycle of the test sequence, actual count intervals corresponding to those listed for the count Interval switch are listed below. Each cycle of the test sequence contains:

Count Interval Switch Setting	Actual Count Interval
10^6	1.048575×10^6 bits
10^7	1.048575×10^7 bits
10^8	1.048575×10^8 bits

1,048,575 bits, as explained in Section 4.2.2 on the Sequence Generator. Thus, count intervals are acutally based on this quantity.

The two decade counters of the Count Interval Control are reset by the main reset line derived from the Display/Count Control. This line also resets the Display Counter.

4.3.22 Display Interval Timer (A12)

Timing for each display interval is supplied by a unijunction-type timer with a logic level inhibit and a logic level output. Two transistors, Q2 and Q3, are connected as the programmable unijunction device. Q1 inhibits operation of the timer by shorting capacitor C3 during the count interval. Q4 serves as a logic level output buffer.

The display interval can be varied from approximately one to ten seconds by means of the Display Interval potentiometer on the front panel. Switching the Display Interval control to "Continuous" operation opens the timer's charging path.

4.3.23 Display/Count Control (A12)

Two flip-flops, IC's 20B and 29, with several gates regulate the gating of errors to the Counter and the resetting of all counters by synchronizing to the Word-Sync, End-of-Count, and End-of-Display signals. At the start of each count interval, the word-sync pulse forces flip-flop IC29, through inverter IC26, to drop time reset line and set count flip-flop IC20B. The count flip-flop, in turn, disables the Display Timer through Q1, opens error gate IC14, and turns on the front panel COUNT indicator. At the end of the count interval, the count flip-flop is reset, reversing the preceding step. The Display Timer then begins to time out unless the DISPLAY INTERVAL countrol is set on "HOLD".

At the end of time-out, flip-flop IC29 sets and causes all counters to reset to zero. They remain reset until the next word-sync pulse starts a new count cycle. Each count interval is synchronized to the Sequence Generator by the word-sync pulse, as described.

Operating the RESET/RESYNC button at any time produces the same result as the time-out pulse from the Display Timer.

4.3.24 Error Counter (A12)
The Error Counter is a two decade arrangement, IC27A and 28A. There is also an overflow flip-flop, IC29A. Both the counters and the overflow flip-flop are reset by the main reset signal from the Display/Count control.

4.3.25 Block Error (A11)
The Block Error Circuit, consisting of IC's 9 through 13, IC14, and IC15A and B, generates a blocking signal of 0.3 ms. The purpose of the blocking signal is to inhibit the display counter for a period of 0.3 ms after an error count has been added, a form of error burst protection.

Binary counters IC11, IC12, IC13A form a nine bit counter chain. This counter chain is driven by the 1.544 MHz transmitter clock under the control of NAND gate IC10C. The outputs of the counter chain are decoded by NAND gate IC14 whose output is then sampled by flip-flop IC13B with the inverted transmitter clock output of IC15A. An output from the sampled flip-flop is applied to control gate IC10C. The transmitter clock is thus applied to the counter chain until the counter reaches the binary number equal to the binary code of the decoder. This establishes the quiescent state of the circuitry. The blocking signal is created each time an error is detected provided the quiescent state exists. Execution is accomplished by resetting the counter chain to zero, resulting in re-application of the transmitter clock. The 0.3 ms blocking signal is measured from zero reset to the acquisition of the decoder output signal.

The reset is controlled by an output from NAND gate IC10B which steers inverted errors from IC10A to the counter reset input when signaled by IC13B that the counter circuit is in its quiescent state. In essence this reset signal is a protected error in that errors which follow within a period of 0.3 ms will not produce a reset signal. The output of IC10B is inverted by IC10D and applied to one input of IC9B. NAND gates IC9A through D are wired to steer either errors or the 0.3 ms protected errors to the display counter, depending on the setting of the switch on the front panel.

4.3.26 Display (A14)
The Display consists of three LED displays with their decoder/drivers (IC1, IC3, IC5). The six front panel indicator lamps are also solid state. All light-emitting-diodes are seven segments for numerals and single segment for the indicators.

CHAPTER 5

MAINTENANCE

5.1 General

Routine care of the Test Set involves simply a periodic calibration. However, should a malfunction be suspected, a performance check is in order. And if a malfunction is definite, the Test Set must undergo troubleshooting procedure. This chapter presents separate sections on calibration, performance check, and troubleshooting. While the first two items are necessarily set procedures, the troubleshooting procedure is a suggested item and a guide. Whether or not the troubleshooting procedure is followed, the responsible technical authority is advised to read it through prior to commencing any investigation.

5.2 Test Equipment Requirements

a.	Frequency Counter	GR Model 1191 or equivalent
b.	Oscilloscope:	Tektronix Model 547 or equivalent
c.	Oscilloscope Accessories:	Tektronix Model 1A1 Plug-In or equivalent, with 2 each X10 Probes and 1 each X1 Probe (calibrate these items to be compatible with the Oscilloscope to be used).

d. BNC to BNC Coaxial Cable

e. Patch Cord with WE-310 type plug at each end

f. Bell System J98710R T-1 Quasi Random Signal Source

g. Tapped Termination, 1 each, per Figure 1

h. Cable Simulator, 1 each, per Figure 2

i. 24 dB Attenuator, 1 each, per Figure 3

j. Termination, 3 each, per Figure 4

k. Test Transmitter: Bowmar/ALI No. D271-129 or equivalent

l. Test Receiver: Bowmar/ALI No. D271-130 or equivalent

m. Resistor, 100 ohms, 1% with an alligator clip at each end.

n. Standard Error Rate Test Set. This set must first have been qualified for use as an operating standard by (1) successfully passing Self Test requirements of Section 3.2 of the Technical Manual for the Error Rate Test Set, and (2) be certified as having synchronized to a Bell System J98710R T-1 Quasi Random Signal Source without recording errors (3) be certified to insert and detect both errors and violations exclusive of one another.

o. Storage Oscilloscope: Tektronix Model 549 or equivalent with a 1A1 Plug In.

p. D.C. Power Supply: Power Designs Model TW5005 or equivalent.

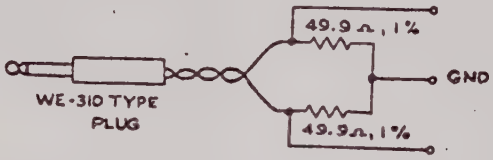


Figure 5-1: Tapped Termination (1 required)

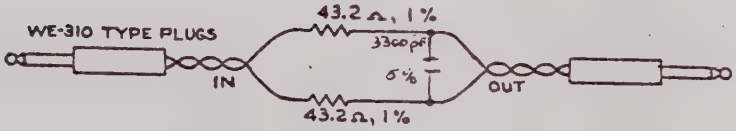


Figure 5-2: Cable Simulator (1 required)

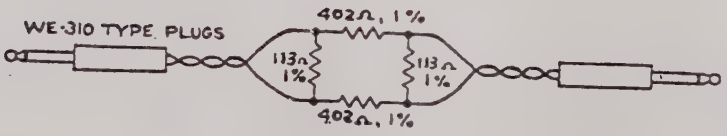


Figure 5-3: 24 dB Attenuator (1 required)

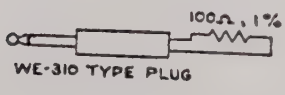


Figure 5-4: Termination (3 required)

5.3 Calibration Procedure

5.3.1 Premiminary

a. Remove the test set from its outer case.

CAUTION: Voltages as high as 115 Vac are present in the vicinity of the Power Switch and the Fuseholder.

b. Apply 115 Vac power to the test set and turn on the Power Switch.

c. Do not connect equipment to the test set except as directed below.

5.3.2 Oscillator Frequency Adjustment

(To be made only after a one-hour minimum warm-up).

a. Connect the Frequency Counter to the TRANSMIT BIT SYNC and GRD terminals on the front panel of the test set.

b. Adjust the Frequency Counter for a one-second count.

c. Adjust capacitor C1, at the read edge of the Transmitter circuit board (A3) for a frequency of 1,544,000 Hz ± 5 Hz.

d. Disconnect the Counter.

5.3.3 Transmitter Amplitude Adjustment

a. Properly calibrate the Oscilloscope, Plug-In, and X10 Probe with respect to both frequency and amplitude using the internal calibration source.

b. Plug the test termination shown in Figure 5-1. of the four output jacks of the Test Set.

c. Connect an X10 Oscilloscope probe between the GRD terminal and either one of the remaining terminals of the Tapped Termination (Figure 5-1).

d. Set the Oscilloscope sweep for 0.1 μsec/cm and vertical sensitivity for 0.05V/cm. Adjust potentiometer R6 (+5V Adjust), on the upper edge of the Power Supply board, for a pulse height of 1.5V (3 cm) ± 0.1V peak or 3.0V (6 cm) ± 0.2V peak as shown in Figure 5-5.

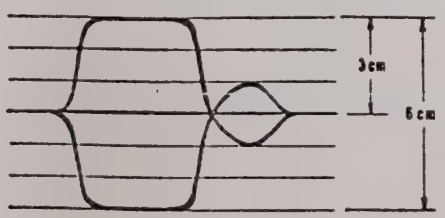


Figure 5-5: Transmitter Amplitude

e. Disconnect the Oscilloscope Probe and unplug the test termination from the Transmitter output jack.

5.3.4 Clock Extractor Timing Adjustment

a. Set up the Oscilloscope as follows:

Plug-In	MODE: CH1 INPUT SELECT: DC VOLTS/CM: 0.2V/CM
Time Base A	
Mode:	Trig
SLOPE:	-
COUPLING:	AC LF Rej
SOURCE:	EXT.
TIME/CM:	0.1 µs/cm
Horizontal Display:	A
Sweep Magnifier:	X1 OFF

b. Using the X1 Probe, connect the TRANSMIT BIT SYNC, on the front panel of the test set to the EXTERNAL SYNC input of the Oscilloscope. Connect the Probe's ground lead to the GRD jack on the front panel of the test set.

c. Using the X10 Probe, connect TP2 on the Receiver circuit board (end board) of the test set to the CH1 input of the Oscilloscope Plug-In. Connect the ground lead of the Probe to the edge foil of the circuit board.

d. Use a tuning tool to adjust inductor L1 on the Receiver board for a symmetrical square wave with clean transitions.

e. Switch the Sweep Magnifier to X10 and adjust the Oscilloscope's position controls to bring a transition into view (See Figure 5-6).

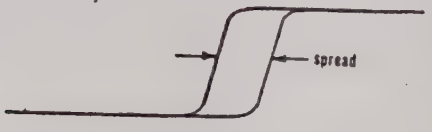


Figure 5-6: Transition Adjustment

g. Continue to adjust L1 for minimum spread on the transition edge, using the Oscilloscope's position controls to keep the pattern centered or conveniently located.

h. Remove the Oscilloscope probes from the test set.

5.3.5 Clock Extractor Phase Adjustment

a. Set up the Oscilloscope as follows:

Plug-In	MODE:	ALT
	INPUT SELECT:	DC
	VOLTS/CM:	0.2V/CM
Time Base A	MODE:	TRIG
	SLOPE:	-
	COUPLING:	AC LF REJ.
	SOURCE:	EXT.
	TIME/CM:	0.1 µs/cm
	Horizontal Display:	A
	Sweep Magnifier:	X5

b. Connect a coaxial cable with BNC connectors between the TRIGGER OUT jack of the Plug-In to the EXT input of TIME BASE A.

c. Using two calibrated X10 Probes, connect CH1 of the Plug-In to TP3 and CH2 to TP2, both on the Receiver circuit board (center board) of the test set.

d. Adjust the position controls and the TIME/CM vernier of the Oscilloscope to obtain the pattern of Figure 5-7, with the upper trace symmetrically positioned.

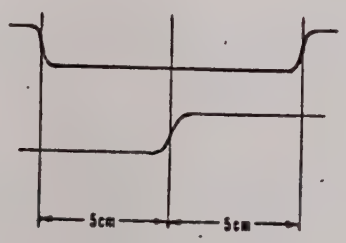


Figure 5-7: Clock Extractor Phase Adjustment

e. Adjust capacitor C11, on the Receiver board (end), to position the lower trace at the center of the upper trace.

f. Disconnect the Oscilloscope from the test set.

5.3.6 Time Base Generator Adjustment

a. Connect the counter between ground to TP1 on the Violations Board A11 and attach to foil.

b. Set the counter controls for a period measurement.

c. Adjust R2 until a measurement of 3.24 ± .01 ms is achieved.

5.3.7 Final

a. Return the test set to its case and secure with the four rear screws.

b. Perform the Self Test (Chapter 2) as a final check of the instrument.

5.4 Performance Checks

5.4.1 Preliminary

These checks are to be made with the Test Set in its case. They may serve for periodic maintenance, quality control checks, and for post-repair checkout. The Error Rate Test Set must be connected to a power source of 115 VAC ± 10%, 50 to 60 Hz.

5.4.2 Transmitter Checks

5.4.2.1 Transmitter Clock Frequency

a. Allow the Test Set to temperature stabilize by operating for at least one hour at room temperature. The Test Set may be momentarily unplugged only for the purpose of moving it.

b. Connect the Counter input to the TRANSMITTER BIT SYNC jack and the GRD terminal located in the lower left section of the front panel.

c. Adjust the Counter for a one-second count interval (to read directly in Hz), and set the Counter's input controls for a consistent display. The Counter should register between 1,543,950 and 1,544,050 at the end of each count interval.

d. Disconnect the Counter.

5.4.2.2 Bipolar Output

a. Check calibration of the Oscilloscope and a X10 probe with respect to frequency compensation and gain, using the internal calibration source of the Oscilloscope and the Oscilloscope manufacturer's procedure.

b. Connect the cord of the test circuit shown in Figure 5-1 to one of the DS-1 Output jacks of the Test Set, and insert the three Terminations (Figure 5-4) into the remaining output jacks. Attach the GRD lead of the X10 probe to the GRD, center, tap of the test circuit and the probe tip to either of the outer taps.

c. Adjust the Oscilloscope for a vertical sensitivity of 0.05V/division and a sweep-rate of 0.1 μsec/division (magnifier off). Adjust the trigger, intensity, and position controls to obtain the waveform shown in Figure 5-8.

d. The measurements designated (1) and (2) in Figure 5-8 should be between 2.7 and 3.3 cm (1.35 and 1.65 volts). Measurements (1) and (2) should differ by not more than 0.15 cm (0.075 volts.)

e. Measurements (3) and (4) should be between 3.0 and 3.5 cm (300 and 350 nsec). Measurements (3) and (4) should differ by not more than 0.15 cm (15 nsec).

f. Measurements (5) and (6), taken between 10% and 90% of peak points, should be less than 0.8 cm (80 nsec).

g. Measurement (7) should be between 10% and 30% of the base line to peak reading (norminally 0.3 to 0.9 cm for a 3.0 cm peak).

h. Measurement (8), taken 4.0 cm to the right of the point of measurement (7), should be less than 10% of measurement (7) (note: It may be necessary to increase the vertical sensitivity in order to make this measurement).

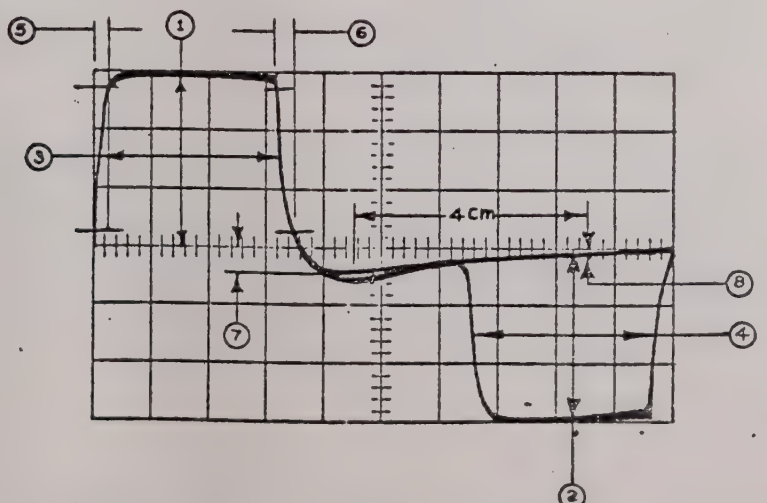


Figure 5-8: Bipolar Waveform

i. Exchange output jack connections with the Tapped Termination and one of the three other Terminations. Repear steps d through h, above.

j. Repeat step i, using a new output jack for the Tapped Termination.

k. Repeat step j. The Tapped Termination should now have been used in all four output jacks.

l. Remove the three terminations one at a time observing the Oscilloscope trace. The trace should not be altered as the terminations are removed. Finally, move the Tapped Termination to one of the three other output jacks. The waveform of Figure 5-8 should re-appear on the Oscilloscope.

m. With no connection to the DS-1 Input jack, momentarily operate the SELF TEST switch to both INTERRUPT DATA and INSERT ERRORS while observing the Oscilloscope.

n. The Oscilloscope waveform should remain unchanged. Disconnect the Tapped Termination from the Test Set.

5.4.2.3 Pattern Content and Error Insertion

a. Connect the Patch Cord between one of the Test Set's outputs and the input of the Standard Test Set (called out under Test Equipment Requirements).

b. Set controls for the Standard Test Set as follows:

MODE	ERRORS
SYNC MODE:	AUTO
DISPLAY INTERVAL:	1 Second
COUNT INTERVAL:	10^6 Bits

c. The NO DATA and NO SYNC indicators of the Standard Test Set should be off, and its Display should be reading a continuous '000'.

d. Set the MODE switch of the Test Set under check to ERRORS and hold its SELF TEST switch at the INSERT ERRORS position. The Display of the Standard Test Set should count to a final reading of '008' at the end of each full count interval. (to the eye, the display may appear to count by '002's).

e. Set the MODE switch of the Test Set under check to VIOLATIONS and continue holding its SELF TEST switch at INSERT ERRORS. The standand Test Set's Display should clear to, and remain at, '000'.

f. Set the MODE switch of the Standard Test Set to VIOLATIONS and continue holding the SELF TEST switch of the Test Set under check at INSERT ERRORS. The Standard Test Set's Display should count to a final reading of '008' at the end of each full count interval. (To the eye, the display may appear to count by '002's).

g. Set the MODE switch of the Test Set under check to ERRORS, and continue holding its SELF TEST switch at INSERT ERRORS. The Standard Test Set's Display should clear to '000'.

h. Release the SELF TEST switch, and remove the Patch Cord connection.

i. Set controls of the Storage Oscilloscope as follows:

Vertical V/cm:	0.1 V/cm
Upper Screen Storage:	Store
Lower Screen Storage:	Store
Screen Selector:	Full
Auto Erase:	Off
Time/cm A:	2 µsec/cm
Horizontal Display:	A, Single Sweep
Magnifier:	Off
Triggering Mode:	Trig
Slope:	- (negative)
Coupling:	AC LF REJ
Source:	EXT.

j. Connect a X1 probe to the Trigger input of the Storage oscilloscope. Insert the probe tip (preferably using a spring tip) into the TRANSMIT WORK SYNC jack of the Test Set. Attach the probe's ground lead to the GRD Terminal on the front panel of the Test Set.

k. Connect the two outputs of the D.C. Power Supply (s) at 5.7 ± 0.2 Vdc, to the Power Input jacks of the Test Receiver (see Test Equipment Requirements list, Section 5.2). Connect a Patch Cord between Input jack of the Test Receiver and a DS-1 output of the Test Set.

l. Connect a X10 Oscilloscope probe between the input of the Storage Oscilloscope and the Output and GRD terminals of the Test Receiver.

m. Operate the Level and Stability controls and the Erase and Reset button of the Oscilloscope to obtain the waveform of Figure 5-9. The waveform should appear each time the push-button is operated. Observe the waveform carefully; it should contain fourteen time slots in which there are no pulses. Also Measurement (1) as measured from the beginning of the pulse train (measuring one time slot), should be between 0.3 and 0.5 cm. (600 and 1000 ms.)

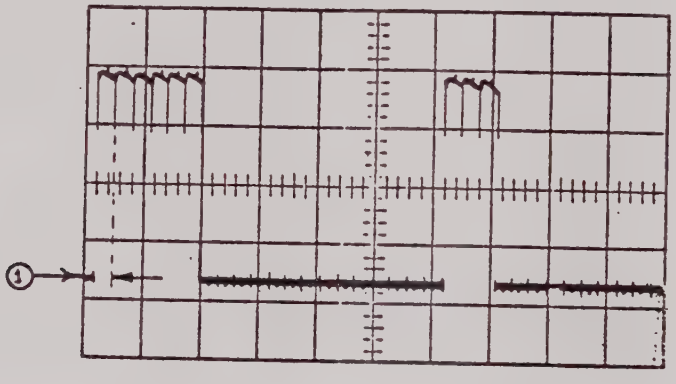


Figure 5-9: Typical 14-zero Condition With No Errors

n. Hold the Test Set's SELF TEST switch at INSERT ERRORS, with the MODE switch in its ERRORS position.

o. While holding the SELF TEST switch, press and release the Oscilloscope's ERASE/RESET button. Again, carefully note the waveform. A pulse displayed earlier at the left of the screen should have disappeared, while another pulse has appeared such that there are now only thirteen time slots with no pulses. These conditions are shown in Figures 5-9 and 5-10. Also, measurement (1) , as measured from the beginning of the trace, should be between 0.3 and 0.5 cm (600 and 1000 ns).

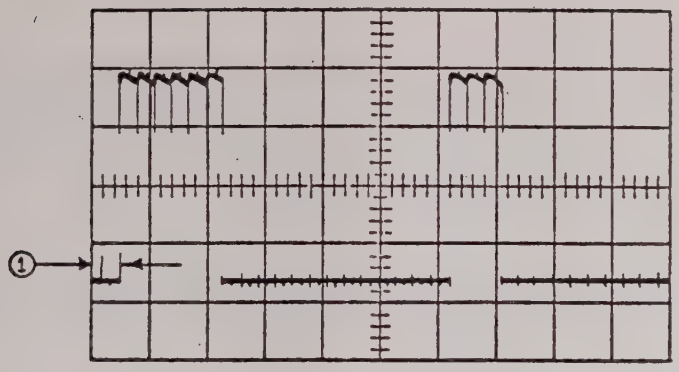


Figure 5-10: Typical 13-zero Condition With two Errors

5.4.3 Receiver Checks

5.4.3.1 General Functional Check

a. Perform the complete Self Test Procedure (see Chapter 2).

b. Return all Test Set controls to the initial switch positions specified in Section 2.2.1, under Self Test Procedure.

5.4.3.2 Receiver Sensitivity to Level and Data Content

a. Connect the input plug of the Cable Simulator (Figure 5-2) to one of the Test Set's DS-1 output jacks, while connecting the input plug to the Test Set's input jack. The NO DATA indicator should be off, and the Display should read '000' at all times.

b. Remove the Cable Simulator, and insert the 24 dB Attenuator (Figure 5-3) in its place. The 24 dB Attenuator is a symmetrical circuit, so that it has no requirement for input and output designations for its plugs. The NO DATA indicator should be off, and the Display should read '000' at all times.

c. Hold the Test Set's SELF TEST switch at its INTERRUPT DATA position. The NO DATA indicator should remain off.

d. Release the SELF TEST switch and remove the 24 dB Attenuator. Connect the two outputs of the DC Power Supply, set for 5.7 $\pm$ 0.2 Vdc to the Power Input jacks of the Test Transmitter (see Test Equipment Requirements list, Section 1.0). Connect a 24 dB Attenuator between the Output jack of the Test Transmitter and the DS-1 input jack of the Test Set.

e. Set the Test Transmitter's rotary switch to its '16' position. In this position, the Test Transmitter provides a bipolar pattern of a single '1' followed by fifteen '0's provided its Reset button has not been actuated. When the Reset button is pressed the Test Transmitter provides an all '0' signal.

f. Press and hold the Test Transmitter's Reset button. The NO DATA indicator, on the Test Set, should go on immediately (in less than 100 msec).

g. Release the Reset button. The NO DATA indicator should go off. The Display should read '000' at all times.

h. Set the Test Transmitter's rotary switch to its '31' position. In this position, the Test Transmitter provides a bipolar pattern of a single '1' followed by thirty '0's, provided its Reset button has been pressed and released.

i. Press and hold the Test Transmitter's Reset button. The NO DATA indicator, on the Test Set, should go on immediately (in less than 100 msec).

j. Release the Reset button. The NO DATA indicator should go off.

k. Set the Test Transmitter's rotary switch to its '50' position. In this position, the Test Transmitter provides a bipolar pattern of a single '1' followed by forty-nine '0's, provided its reset button has been pressed and released.

l. Press and hold the Test Transmitter's Reset button. The NO DATA indicator on the Test Set should go on immediately (in less than 100 msec).

m. Release the Reset button. The NO DATA indicator should remain on.

n. Set the Test Transmitter's rotary switch to its all 1's position. Observe that the all 1's indicator on the test sets front panel is illuminated (actuated).

5.4.3.3 Auxiliary Output Checks

a. Remove any connection from the Test Set's DS-1 input jack, and set front panel controls as follows:

MODE:	ERRORS
SELF TEST:	NORMAL
SYNC MODE:	MANUAL
COUNT INT:	CONT.

b. Set the Oscilloscope controls as follows:

Vertical (V/cm):	0.1 V/cm
Coupling (Voltage):	D. C.
Time Base:	0.1 usec/cm
Triggering Mode	TRIG
Triggering Slope:	- (negative)
Coupling (Trigger):	AC LF REJ
Source:	NORM

c. Connect the ground lead of a properly calibrated X10 probe to the Test Set's front panel GRD terminal, and connect the probe tip (using a spring tip) to the Test Set's TRANSMIT BIT SYNC jack.

d. Adjust the Oscilloscope's trigger level and position controls for the waveform of Figure 5-11. Measurement (1) should be between 4.5 and 5.5 cm (4.5 and 5.5 volts.) Measurement (2) should be between 3.0 and 3.5 cm (300 and 350 nsec). Measurements (3) and (4), taken at the 10% and 90% points, should be less than 0.5 cm (50 nsec).

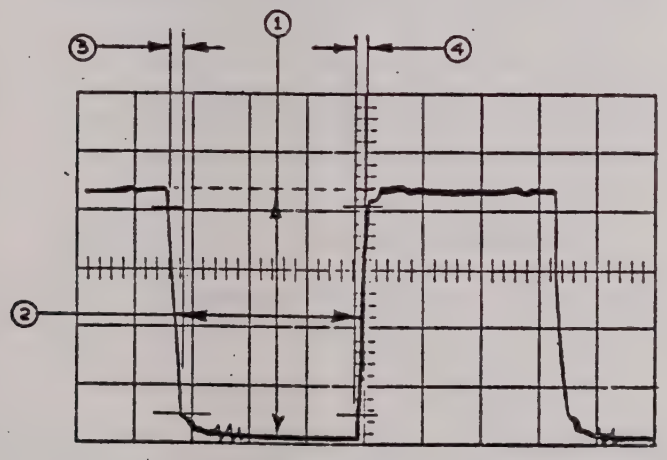


Figure 5-11: Transmit Bit Sync

e. Using the 100 ohms, 1% Resistor whose ends are wired to alligator clips, fasten the Resistor between the probe's tip and the GRD terminal. Measurement 1 of Figure 5-11 should now be not less than one half of Measurement (1) taken in the previous step.

f. Remove the probe tip and resistor from the TRANSMIT BIT SYNC jack. Insert the probe without Resistor into the RECEIVE BIT SYNC jack, and repeat steps d and e, above, using Figure 5-11 and the assigned measurement values.

g. Remove the probe tip and resistor from the RECEIVE BIT SYNC jack. Connect probe tip without resistor into the ERRORS jack. Momentarily push the SELF TEST switch to INTERRUPT Data, to force the Receiver out of synchronization thereby producing a large number of errors.

h. Observe the waveform of Figure 12. Measurement (1) should be between 4.5 and 5.5 cm (4.5 and 5.5 volts). Measurement (2) should be between 3.0 and 3.5 cm (300 and 350 nsec). Measurement (3) and (4), taken at the 10% and 90% points, should be less than 0.5 cm (50 nsec). There may be a small amount (<15%) of ringing on the signal.

i. Using the 100 ohms, 1% resistor whose ends are wired to alligator clips, fasten the resistor between the BNC connector and the GRD terminal. Measurement 1 of Figure 5-12 should now be not less than one half of Measurement (1) taken in the previous step.

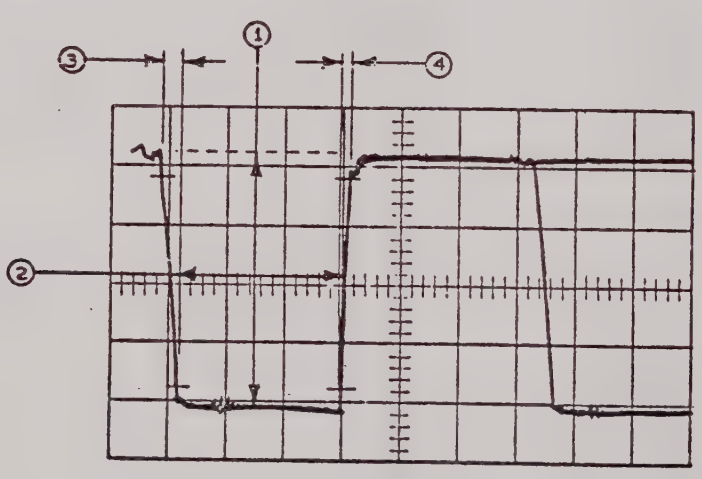


Figure 5-12: Errors

Set controls of the Storage Oscilloscope as follows:

Vertical V/cm:	0.1V/cm
Upper Screen Storage:	Store
Lower Screen Storage:	Store
Screen Selector:	Full
Auto Erase	Off
Time/cm A:	0.1 us/cm
Horizonatal Display:	A, Single Sweep
Magnifier:	Off
Triggering Mode:	Trig
Slope:	- (negative)
Coupling:	AC LF REJ
Source:	NORM

j. Using a properly calibrated X10 probe, connect the probe tip (preferably a spring tip) to the TRANSMIT WORD SYNC jack of the Test Set. Connect the probe's ground lead to the Test Set's GRD terminal.

k. Operate the Storage Oscilloscope's Trigger, storage, and position controls to obtain the waveform of Figure 5-13, after the Erase & Reset button has been momentarily pushed. Measurement (1) should be between 4.5 and 5.5 cm (4.5 and 5.5 volts). Measurement (2) should be between 3.0 and 3.5 cm (300 and 350 nsec). Measurement (3) and (4), taken at the 10% and 90% points should be less than 0.5 cm (50 nsec).

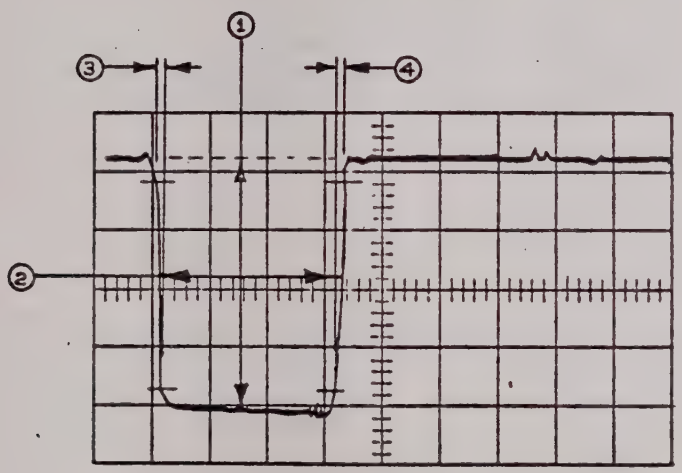


Figure 5-13: Transmit Word Sync

l. Connect the alligator clip of the 100 ohms, 1% resistor between probe tip and ground connection. Measurement 1 from Figure 5-13, should be not less than 2.25 cm and 2.75 cm (2.25 and 2.75 volts).

m. Remove the probe tip and resistor combination from the TRANSMIT WORD SYNC jack. Insert the probe tip only into the Test Set's RECEIVE WORD SYNC jack, and repeat steps k and l, above.

n. Change the Storage Oscilloscope's triggering source control to EXT. Connect a X1 probe to the TRIG INPUT of the Oscilloscope. Connect the X1 probe's tip to the Test Set's TRANSMIT WORD SYNC jack and the probe's ground lead to the Test Set's GRD terminal. Connect the X10 probe between the Oscilloscope's vertical input and the Test Set's TRANSMIT BIT SYNC jack.

o. Adjust the Oscilloscope's triggering controls to obtain the waveform of Figure 5-14. When properly triggered, the Oscilloscope should exhibit a slight delay (not more than 2/3 second) between release of its Erase & Reset button and the actual sweep. Measurement (1) should be between 1 and 3 cm (100 and 300 ns) from the beginning of the trace.

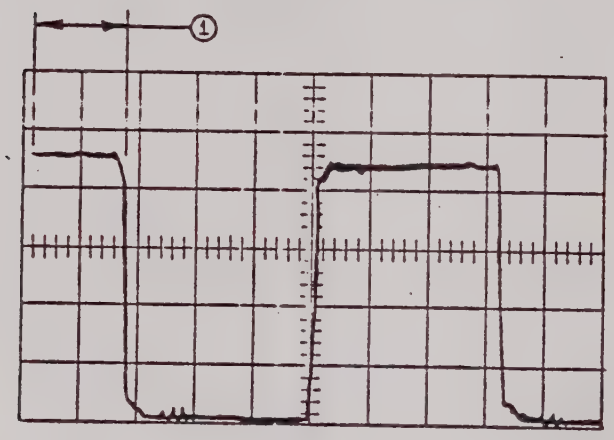


Figure 5-14: Transmit Bit Sync

5.5 Troubleshooting

5.5.1 Preliminary

Unless otherwise specified, the following procedures are to be performed with the Test Set in its case. Their intent is to aid in isolating the cause of malfunction to at least circuit board level.

In some cases, more than one procedure can be used to isolate a problem. The choice may be dictated by availability of test equipment.

Before proceeding, connect the Test Set to a power source of 115 Vac ± 10%, 50-60 Hz. The Test Set's fuse should have been checked and replaced if necessary.

CAUTION: If the Test Set is removed from its outer case, voltages as high as 115 Vac are present in the vicinity of the Power Switch and the Fuseholder.

Do not connect equipment to the Test Set except as directed below.

5.5.2 Power Supply Checks

a. A Power Supply malfunction may be suspected if any of the following conditions exist.

1. The Test Set repeatly blows fuses of the proper size and type (Littlefuse 3AG Slo-Blo Fuse at 1/2 Amp).

2. The Display and solid state indicators are too bright, too dark, or off (while Power indicator remains illuminated).

3. The Transmitter and Receiver simultaneously fails tests outlined in sections that follow.

b. A suspected Power Supply malfunction can be confirmed by removing the Test Set from its outer case and checking the three test points visible through the opening in the right side plate. Voltages at the three test points should be as specified in the table below.

Test Point	Voltage
+5	+4.5 to +5.5 Vdc
-5	-4.5 to -5.5 Vdc
+5 ADJ	+4.5 to +8.5 Vdc

If a short circuit appears likely, remove the plug-in printed circuit boards one at a time while monitoring the shorted supply point. This action should narrow isolation of the short to one of the boards or to the chassis wiring.

NOTE: If the voltages measured above are not within specified limits, the plug-in boards should be removed from the Test Set until repairs are complete.

5.5.3 Transmitter Cross-Check

a. Perform 5.4.2.3 a through h of the Performance Checks entitled Pattern Content and Error Insertion. Any failure indicated by these checks may be attributed to the Transmitter Board, printed circuit card A10.

b. The Transmitter can be further analyzed by checking its bipolar output waveform against the Performance Checks of 5.4.2.2, entitled Bipolar Output.

5.5.4 Receiver Cross-Checks

NOTE: The receiver, error detectors and error counters are to be tested first as an entity although the circuits reside on three different printed circuit boards. Procedures for isolating the malfunction to any one board follow the overall receiver tests. Printed circuit board substitutions can also be used as an isolation technique if a replacement set of boards is available.

a. Connect the Patch Cord between the input of the Test Set under check and one of the outputs of the Standard Test Set.

b. Set the front panel controls of the two Test Sets as follows:

Control	Test Set Under Check	Std. Test Set
MODE:	VIOLATIONS	VIOLATIONS
ERROR BLOCK:	OUT	_____
SELF TEST:	NORMAL	NORMAL
SYNC MODE:	MANUAL	AUTO
COUNT INTERVAL:	10^6	10^6
DISPLAY INT:	FULL CCW (1 sec)	FULL CCW (1 sec)

c. On the Test Set under check the indicators should respond as follows:

NO DATA:	OFF
NO SYNC:	ON
LOST SYNC:	ON
All 1's	OFF
Numerical Display:	'000' at all times
OVERFLOW:	OFF
COUNT:	On for approximately 2/3 sec. Off for approximately 3/4 to 1 1/2 sec.

d. If the Test Set under check operates in SELF TEST, i.e. with no input to the input jack, and not when connected to the standard Test Set or vice versa, the malfunction may be located in the Receiver board, A13, in the connection between the input jack and the A13 board or in the SELF TEST switch.

e. If the NO DATA indicator remains on and the COUNT indicator remains either on or off while signal is being supplied to the input jack, the malfunction is most likely in either the Receiver Module, A13, or the connection between this module and input jack.

f. If the COUNT indicator remains off, momentarily depress the RESET/RESYNC button of the Test Set under check. If the COUNT indicator comes on within 2/3 sec. of the release of this button and remains on for 2/3 sec., the malfunction is most likely in either the DISPLAY INTERVAL control, the connections between the control and the RECEIVER LOGIC board, A12, or the discrete circuitry located on the front end of the A12 card.

g. If the COUNT indicator remains on, momentarily depress the RESET/RESYNC button of the Test Set under check. If the COUNT indicator goes off when the button is depressed and comes on with 2/3 second of the button's release, the malfunction is most likely in either the COUNT INTERVAL control, the RECEIVER LOGIC board, A12, or the connections between the two.

h. Assuming that the NO DATA indicator is off and the COUNT INDICATOR operates as described above, push and hold the SELF TEST switch of the Standard Test Set to its INSERT ERRORS position. The indicated count on the Display of the Test Set under check should clear to a starting count of '00' and progress to a final count of '08' while the COUNT indicator is on. During the counting process, the spacing of errors will cause the Display to appear to be counting by increments of '02'. At the count of '08', the Display should hold for the period set by the DISPLAY INTERVAL control, then it should clear to '00' and begin a new cycle.

i. If the Display of the Test Set under check appears to be counting correctly but that one or more segments are missing from the display, the malfunction is located on the front panel of the Test Set.

j. Change the COUNT INTERVAL control of the Test Set under check from 10^6 to 10^7, and continue holding the SELF TEST switch of the Standard Test Set at its INSERT ERRORS position. The indicated count, on the Display, should perform as it did in Step h above. However, the final count should now be '80'.

k. Change the COUNT INTERVAL control of the Test Set under check from 10^7 to 10^8, and continue holding the SELF TEST switch of the Standard Test Set at its INSERT ERRORS position. The Display should cycle through a complete count of 0 to 100, a total of eight times. Since the Display contains only two digits, a count of 100 will register as '00' with an OVERFLOW indication. Again, spacing of errors will make the Display appear to be counting by increments of '02'.

   The OVERFLOW indicator should come on at the first count of 100. It will remain on after this point, through the remaining seven cycles of 0 to 100. This entire process takes about 70 seconds.

l. Change the COUNT INTERVAL control of the Test Set under check from 10^8 to CONT. The Display and OVERFLOW indicator should behave as in the preceding step (k) except that the Display will continue to cycle through 0 to 100 as long as the count interval is set for continuous running. The Test Set should be checked in this mode for at least 70 seconds.

m. While holding the SELF TEST switch of the Standard Test Set at its INSERT ERRORS position, momentarily press the RESET/RESYNC button. The Display, and the COUNT and OVERFLOW indicators of the Test Set under check should reset. A new count interval should begin within 2/3 second of release of the button.

n. Release the SELF TEST switch of the Standard Test Set and return the COUNT INTERVAL switch of the Test Set under check to its 10^6 position.

o. Set the MODE switch of the Test Set under check for ERRORS and momentarily press the RESET/RESYNC button. The display indication should be '00' at all times, while the NO DATA, NO SYNC, and LOST SYNC indicators should be off.

p. If the NO SYNC indicator does not go off, yet the Test Set detected and recorded violations, the malfunction is most likely located in the RECEIVER LOGIC printed circuit board, the ERRORS/VIOLATIONS switch or the connection between the two.

   NOTE: The out-of-sync condition is indicated by both the NO SYNC indicator and the fact that the Display will show '88' with an OVERFLOW indication during the count interval and any number with OVERFLOW at the end of the count interval.

q. Set the SYNC MODE switch of the Test Set under check to AUTO and remove the patch cord from the input jack of the Test Set under check. The NO DATA and NO SYNC indicators should come on immediately (in less than 100 ms). The LOST SYNC indicator may or may not come on.

r. Reconnect the patch cord removed in the previous step. The NO DATA and NO SYNC indicators should go off. The LOST SYNC indicator should come on if not already on. The Display should show '00' errors.

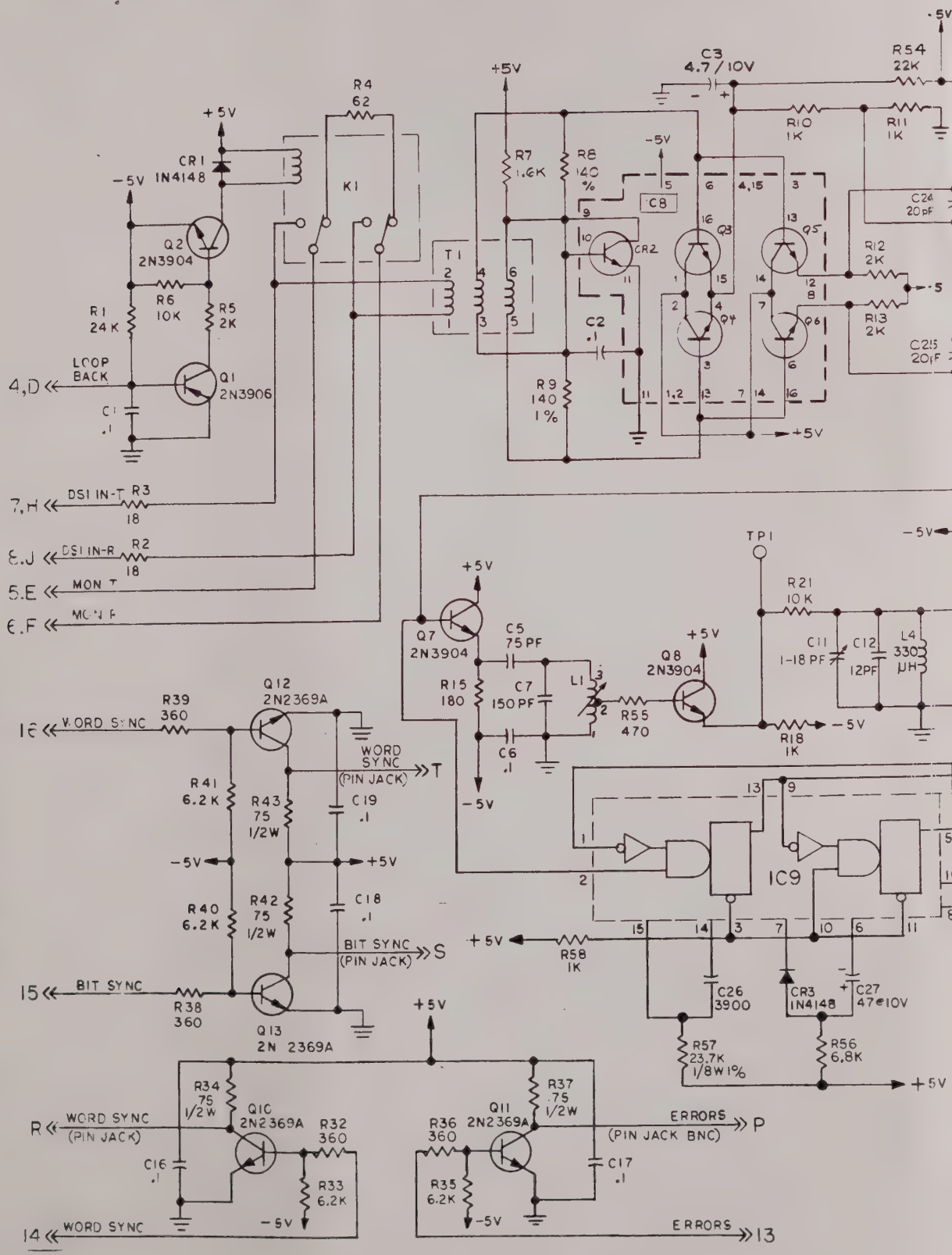
s. Momentarily pressing the RESET/RESYNC button should reset the LOST SYNC indicator and the NO SYNC indicator should remain off.

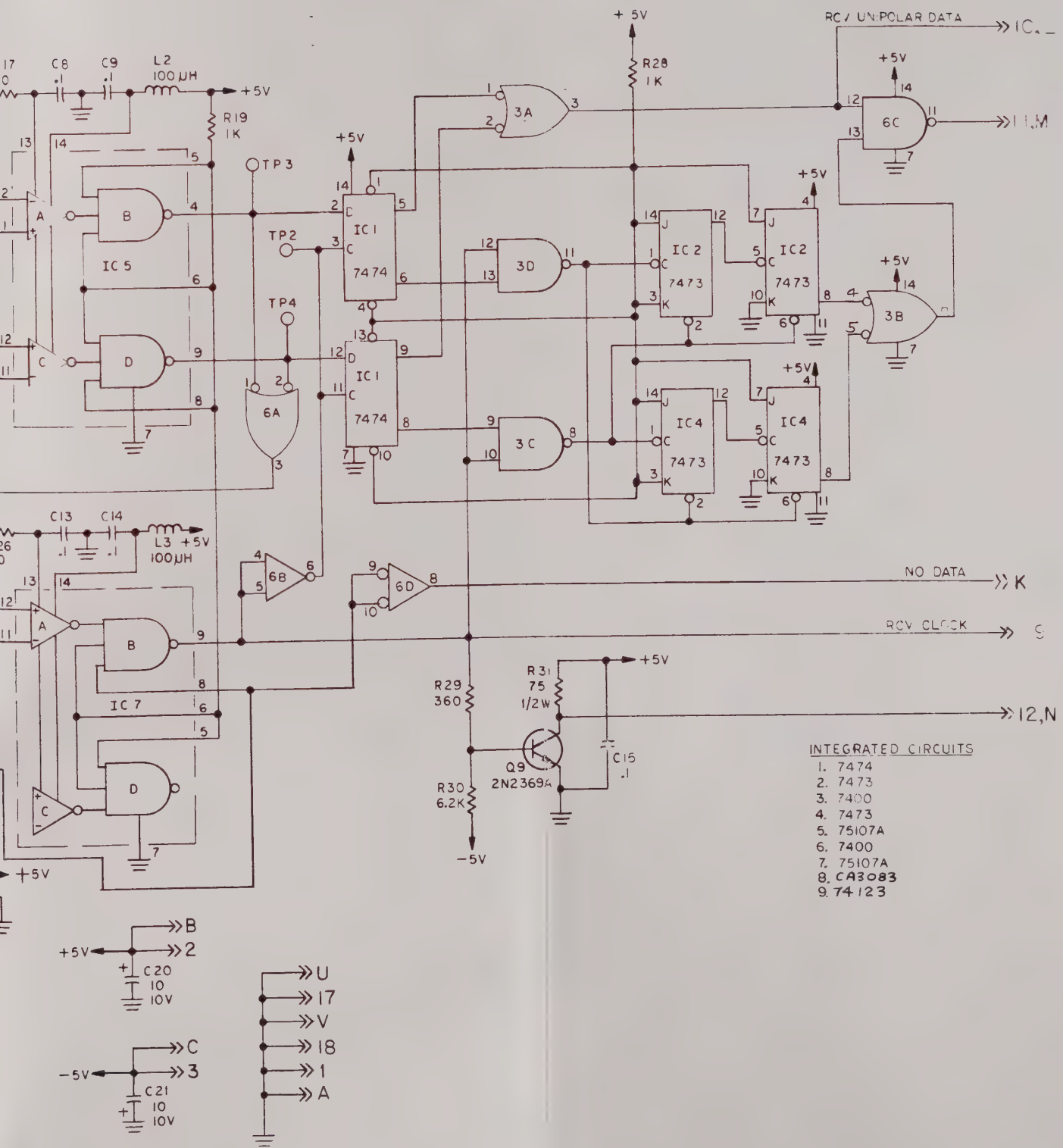
t. Trouble completing the last three steps but not the earlier steps indicates that the malfunction is most liekly in the RECEIVER LOGIC printed circuit board.

CHAPTER 6

DIAGRAMS

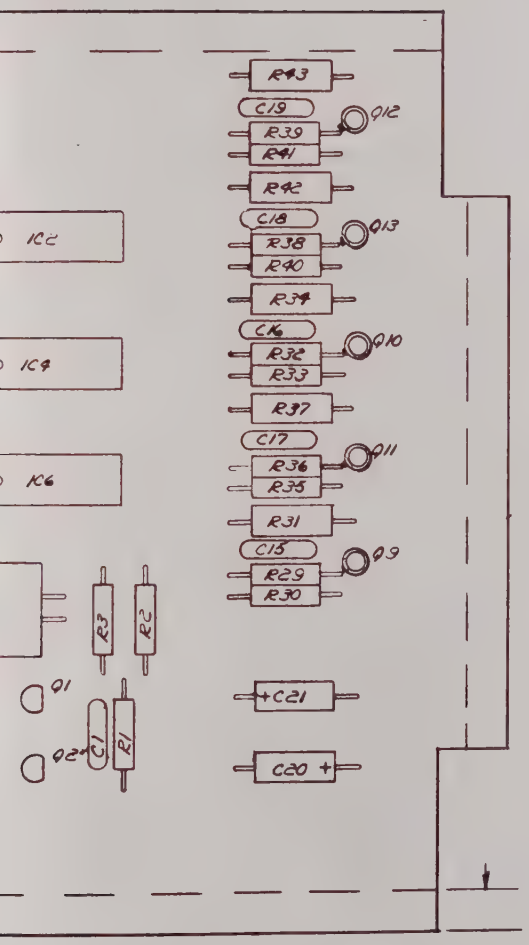
DRAWING TITLE	DRAWING NO.
Receiver Module Schematic	D271-112
Receiver Module Assembly	D271-212
Transmitter Module Schematic	D271-111
Transmitter Module Assembly	D271-211
Power Supply Schematic	D271-104
Power Supply Assembly	C271-204
Interconnection Assembly	C271-214
Display Module Schematic	D271-113
Display Module Assembly	D271-213
Receiver Logic Module Schematic	D271-110
Receiver Logic Module Assembly	D271-210
Violations Schematic	D271-117
Violations Assembly	D271-217
Main Schematic	D271-114
Main Assembly	E271-227


+5V
-5V
R4
62
K1
CR1
IN4148
Q2
2N3904
R1
24K
R6
10K
R5
2K
LOOP
BACK
4,D
Q1
2N3906
C1
.1
7,H
DSI IN-T
R3
18
8,J
DSI IN-R
R2
18
5,E
MON T
6,F
MON R
T1
R7
1.6K
R8
140
%
C8
C2
.1
R9
140
1%
CR2
Q3
Q5
Q4
Q6
C3
4.7/10V
R54
22K
R10
1K
R11
1K
C24
20PF
R12
2K
R13
2K
C21
20PF
TP1
R21
10K
C11
1-18 PF
C12
12PF
L4
330
μH
Q7
2N3904
C5
75 PF
R15
180
C7
150 PF
L1
C6
.1
Q8
2N3904
R55
470
R18
1K
Q12
2N2369A
R39
360
16
WORD SYNC
WORD
SYNC
(PIN JACK)
T
R41
6.2K
R43
75
1/2W
C19
.1
R40
6.2K
R42
75
1/2W
C18
.1
BIT SYNC
(PIN JACK)
S
15
BIT SYNC
R38
360
Q13
2N 2369A
IC9
R58
1K
C26
3900
CR3
IN4148
C27
47@10V
R57
23.7K
1/8W 1%
R56
6.8K
R34
75
1/2W
Q10
2N2369A
R32
360
R
WORD SYNC
(PIN JACK)
C16
.1
R33
6.2K
14
WORD SYNC
R37
75
1/2W
Q11
2N2369A
R36
360
ERRORS
(PIN JACK BNC)
P
C17
.1
R35
6.2K
ERRORS
13

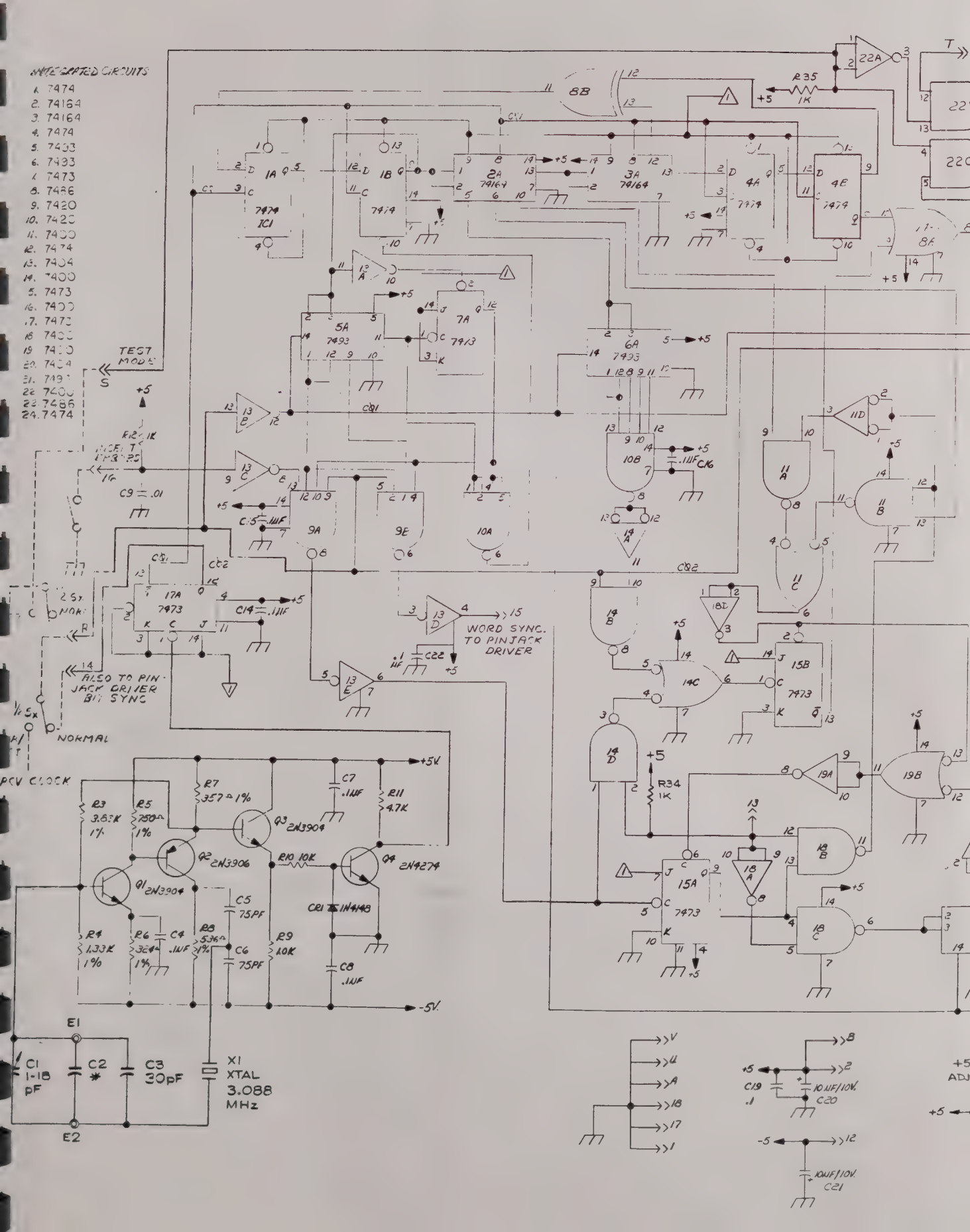


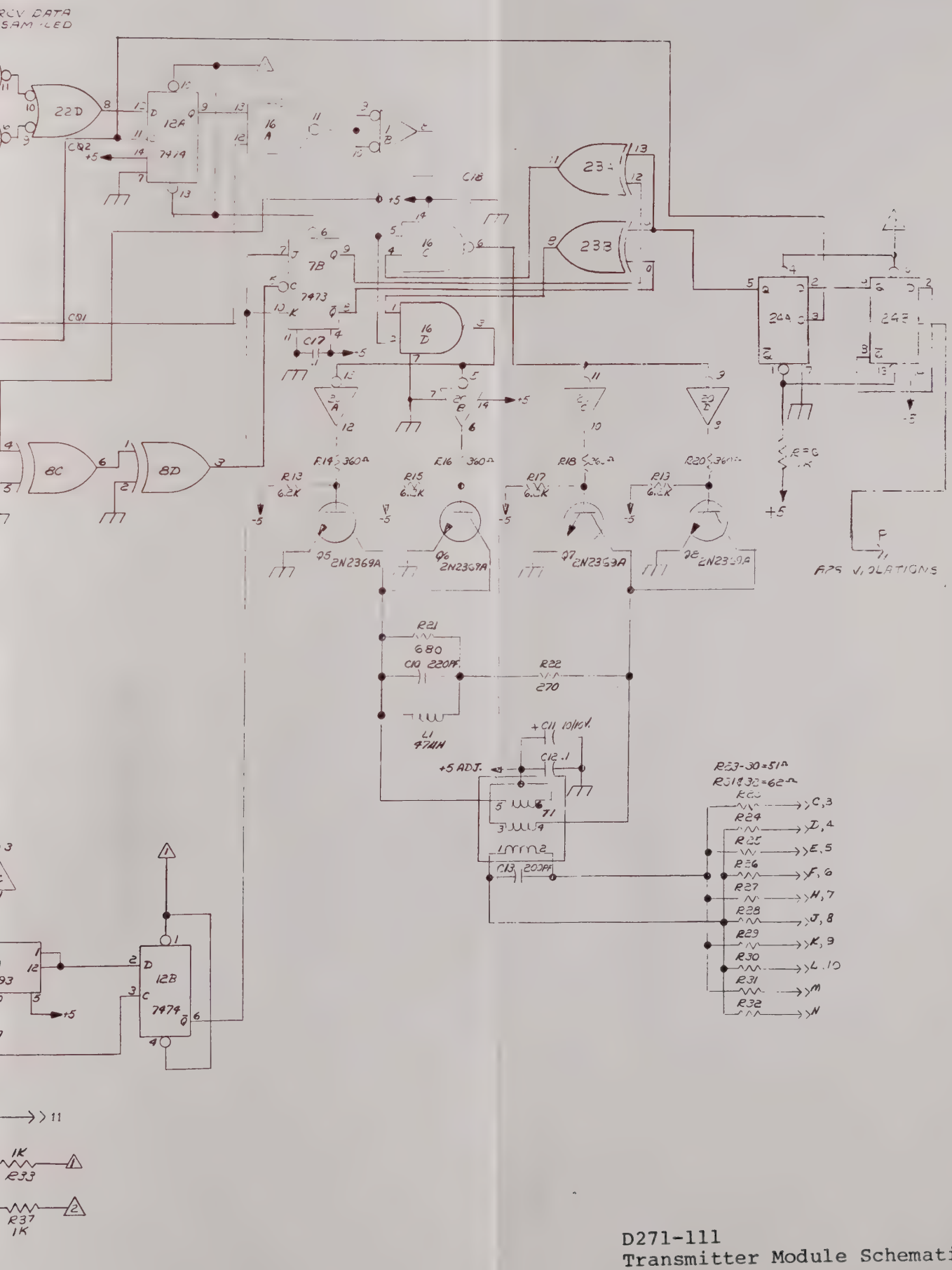
D271-112
Receiver Board Schematic

A
A
D271-212-[ ]/[ ]
C27 +
R58
CR3
R56
R57
C26
C11
L4
C12
IC9
R28
K1
L1
R55
Q8
K7
K3
Q7
R18
C5
C7
C6
R15
R21
C13
R26
C14
L3
C24
K5
IC8
R8
F9
R4
K1
C25
R54
R19
C9
L2
C8
R17
R11
R10
C3 +
R13
R12
C2
R7
6 4 2
T1
5 3 1
R6



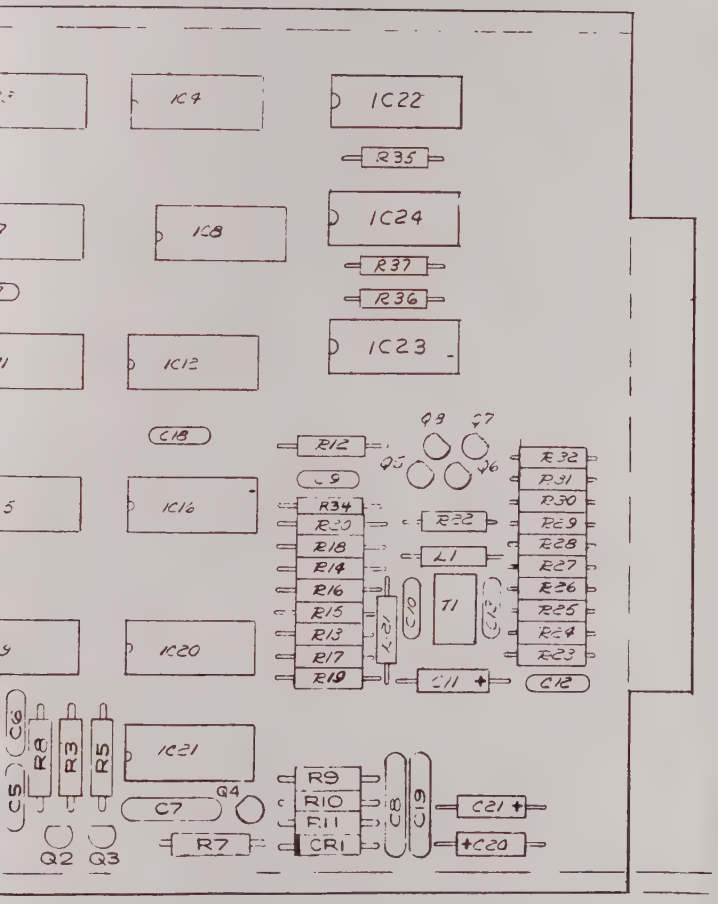
D271-212
Receiver Module Assembly


INTEGRATED CIRCUITS
1. 7474
2. 74164
3. 74164
4. 7474
5. 7493
6. 7493
7. 7473
8. 7486
9. 7420
10. 7420
11. 7400
12. 7474
13. 7404
14. 7400
15. 7473
16. 7400
17. 7473
18. 7400
19. 7400
20. 7404
21. 7493
22. 7400
23. 7486
24. 7474
TEST MODE
S
+5
R12 1K
NORMAL
C9 = .01
C5 = .1UF
C14 = .1UF
ALSO TO PIN JACK ORIER BIT SYNC
NORMAL
PCV CLOCK
WORD SYNC. TO PINJACK DRIVER
C22 .1 UF
R35 1K
R34 1K
+5V
-5V.
R7 357Ω 1%
R3 3.83K 1%
R5 750Ω 1%
R4 1.33K 1%
R6 324Ω 1%
R8 536Ω 1%
R9 1.0K
R10 10K
R11 4.7K
C4 .1UF
C5 75PF
C6 75PF
C7 .1UF
C8 .1UF
Q1 2N3904
Q2 2N3906
Q3 2N3904
Q4 2N4274
CR1 1N4148
E1
E2
C1 1-18 pF
C2 *
C3 30pF
X1 XTAL 3.088 MHz
C19 .1
C20 10 UF/10V.
C21 10UF/10V.
+5 ADJ

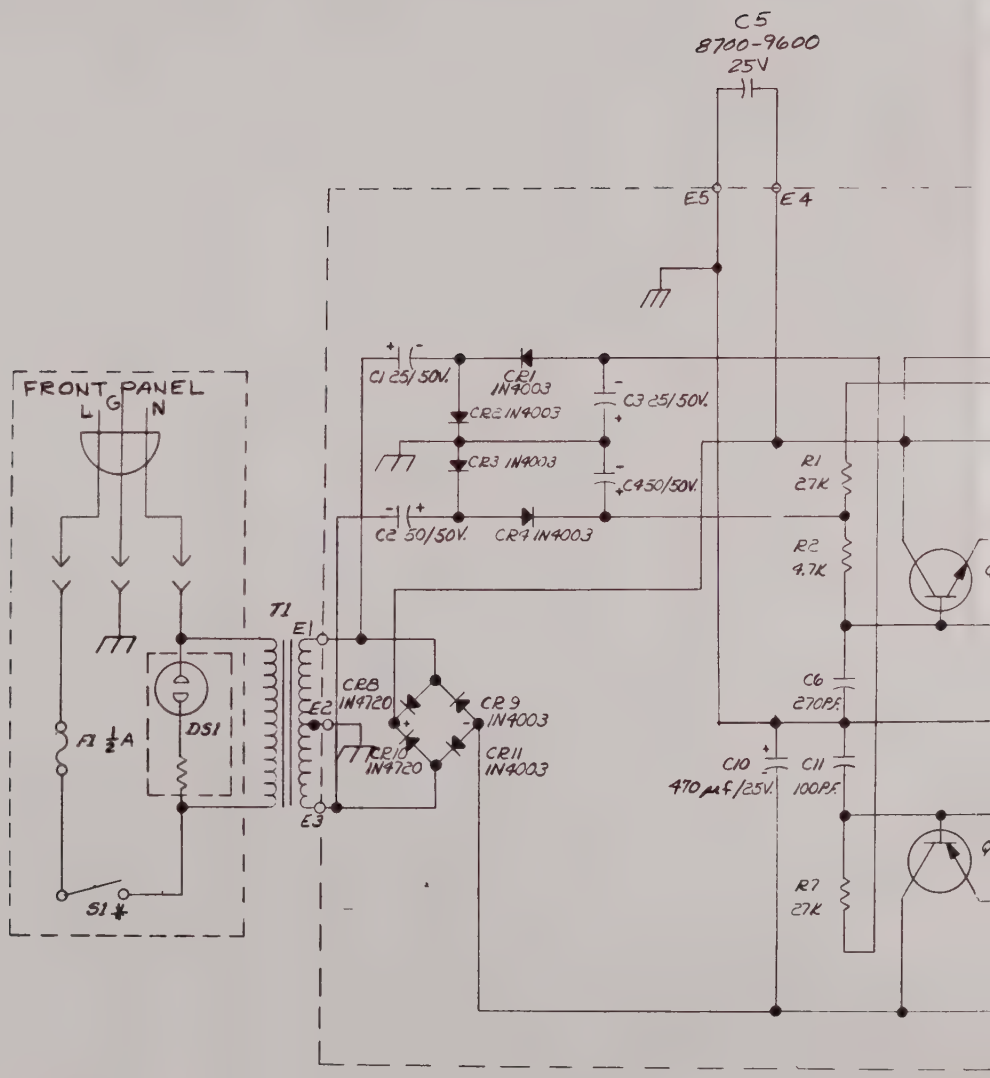


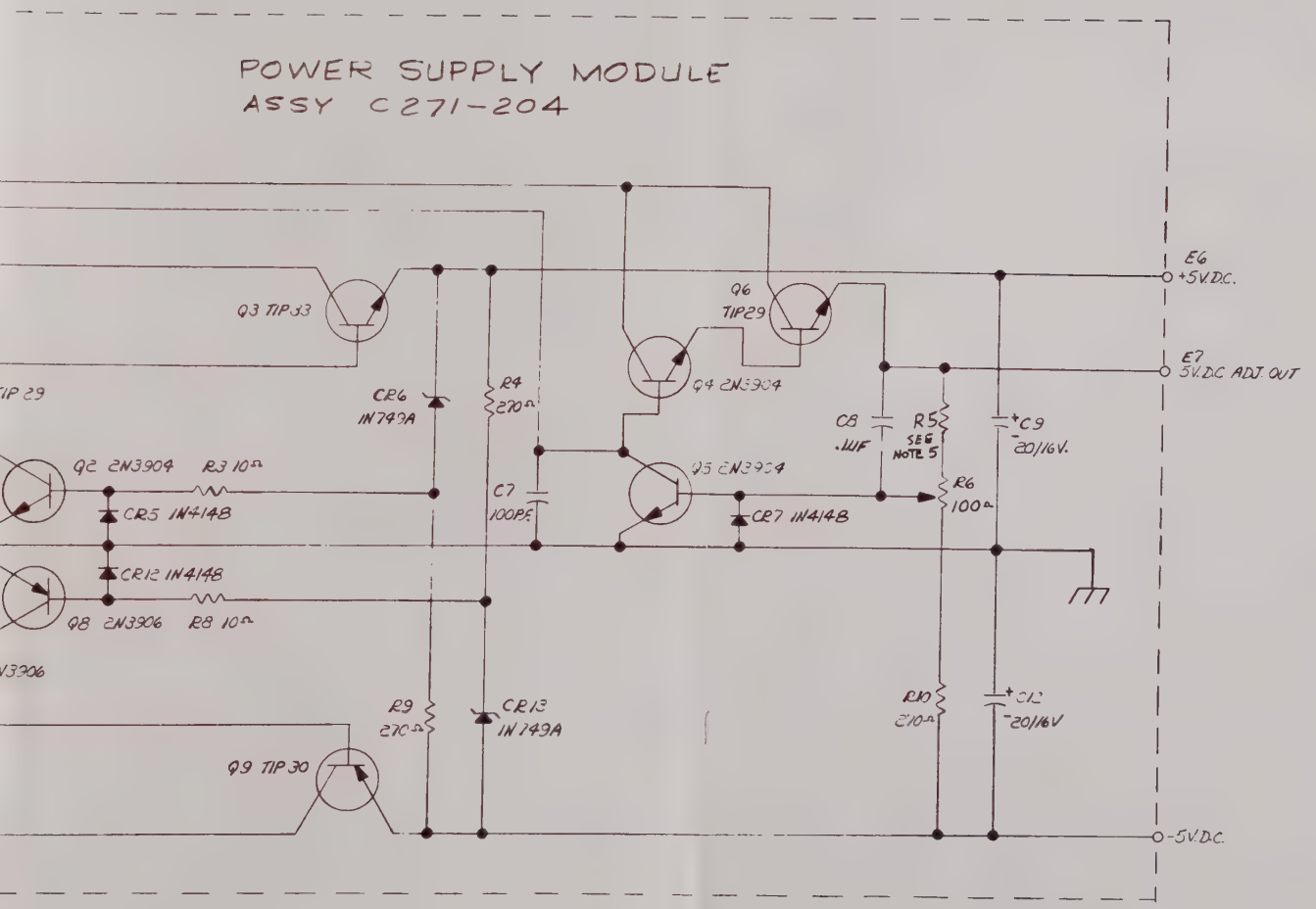
D271-111
Transmitter Module Schematic

D271 211/E
IC1
IC2
R33
IC5
IC6
C15
C16
IC9
IC10
IC13
IC14
C22
IC17
IC18
A
C2
A
C3
C1
X1
R4
R6
C14
Q1



D271-211
Transmitter Module Assembly

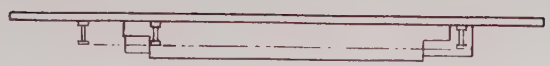

C5
8700-9600
25V
E5
E4
FRONT PANEL
L
G
N
C1 25/50V.
CR1 IN4003
CR2 IN4003
C3 25/50V.
CR3 IN4003
C4 50/50V.
C2 50/50V.
CR4 IN4003
R1
27K
R2
4.7K
T1
E1
E2
E3
CR8 IN4720
CR9 IN4003
CR10 IN4720
CR11 IN4003
C6
270P.F.
C10
470 µf/25V.
C11
100P.F.
R7
27K
F1 ½A
DS1
S1

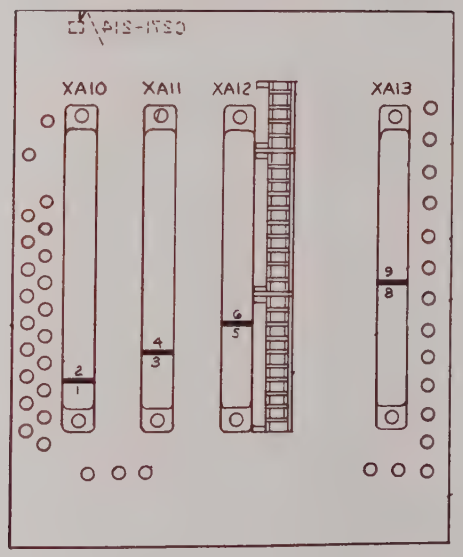


D271-104
Power Supply Schematic

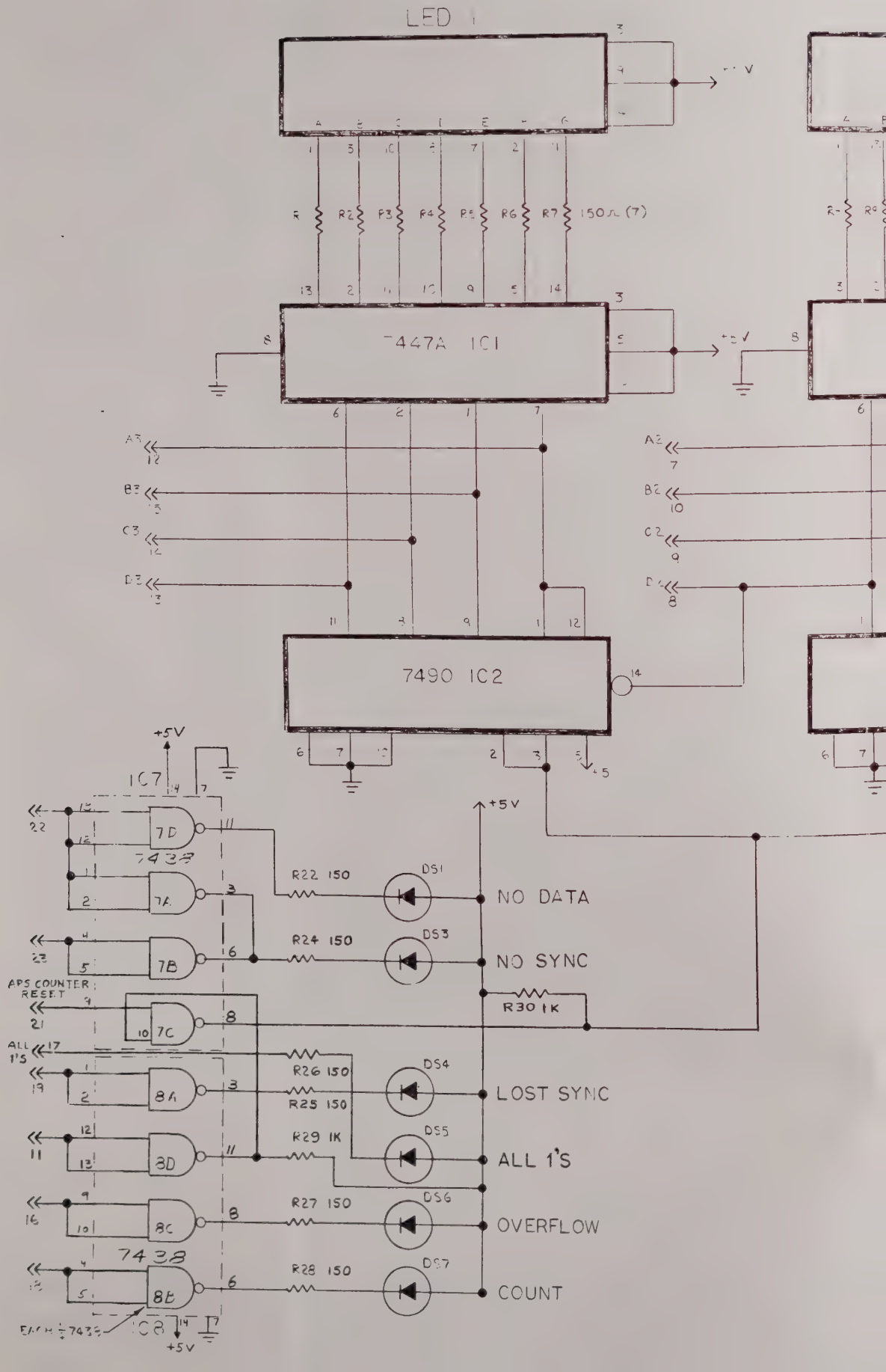
Q9
Q1
Q7
Q8
Q2
CR12
CR13
R9
R8
R7
C11
C6
C10
C3
CR9
CR11
E2
E1

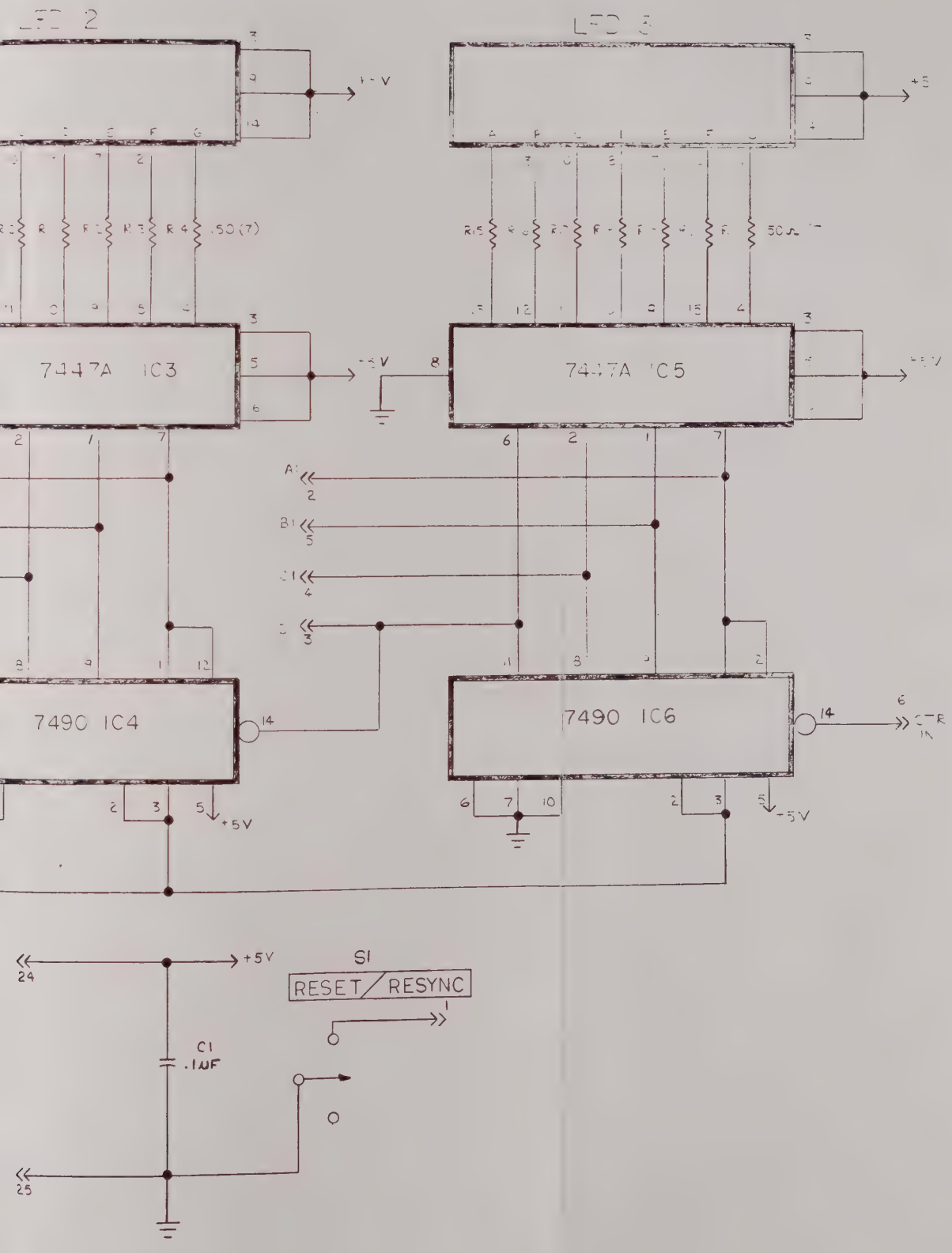
C271-204
Power Supply Assembly



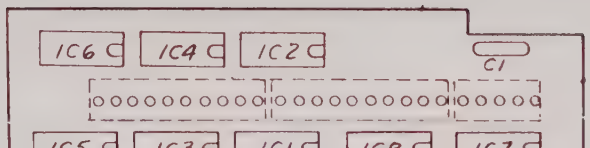


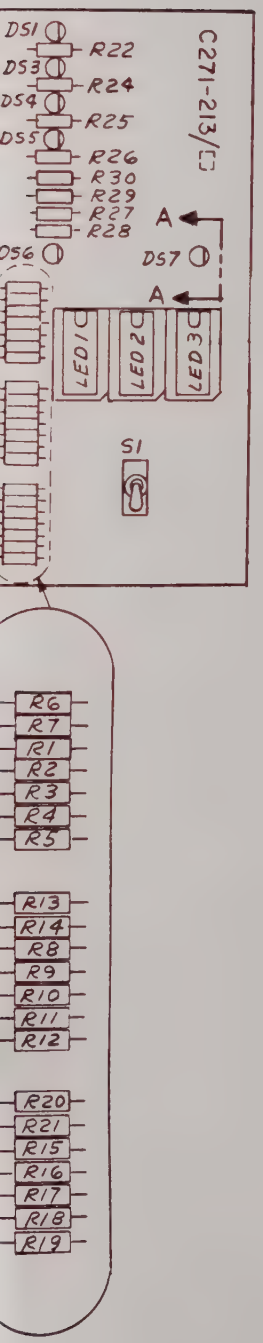
C271-214
Interconnection Assembly


LED
R1
R2
R3
R4
R5
R6
R7
150Ω (7)
7447A IC1
A3
B3
C3
D3
A2
B2
C2
7490 IC2
+5V
IC7
7408
7D
7A
7B
7C
IC8
7438
8A
8D
8C
8B
APS COUNTER RESET
ALL 1'S
R22 150
R24 150
R30 1K
R26 150
R25 150
R29 1K
R27 150
R28 150
DS1
DS3
DS4
DS5
DS6
DS7
NO DATA
NO SYNC
LOST SYNC
ALL 1'S
OVERFLOW
COUNT

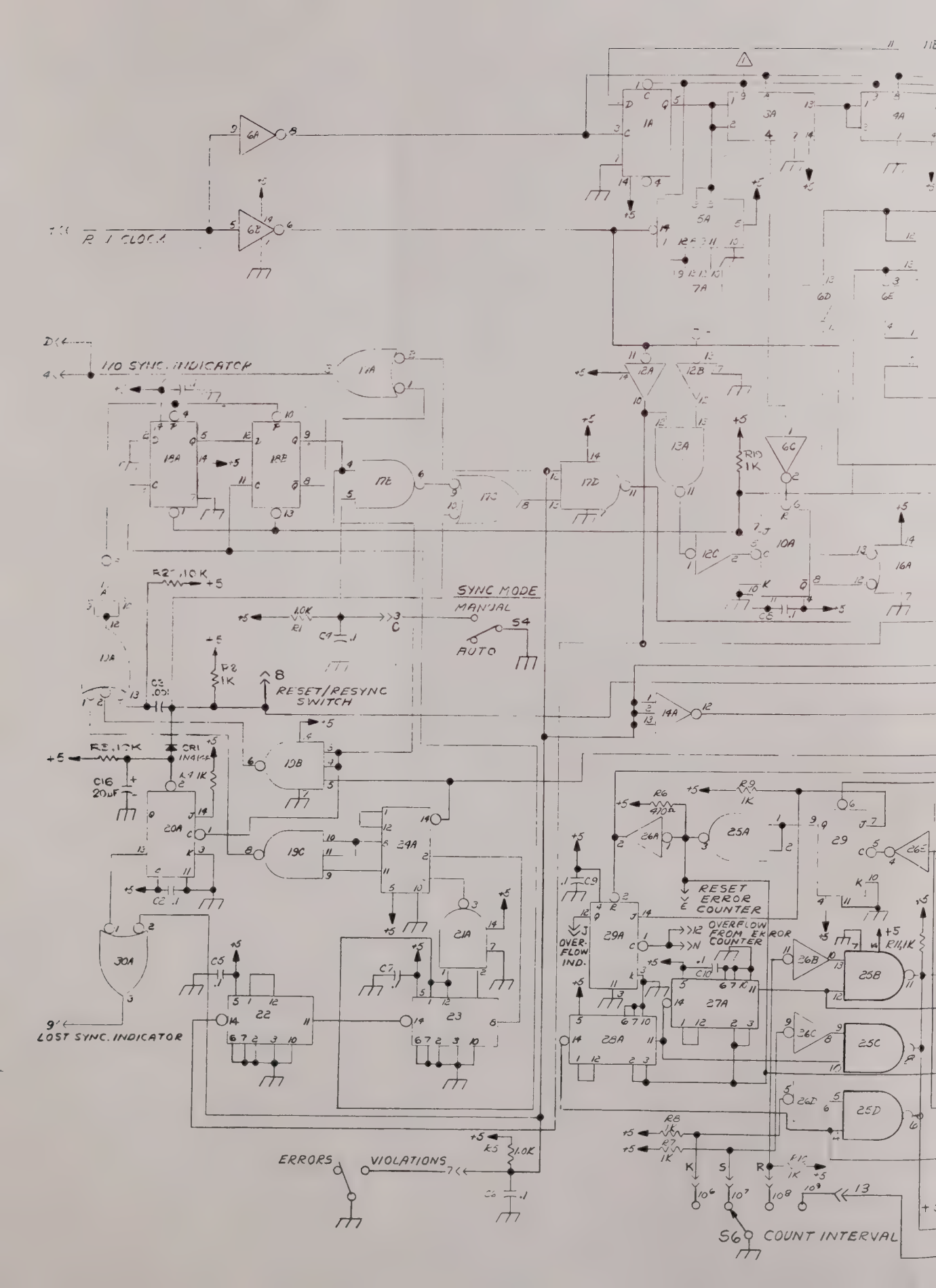


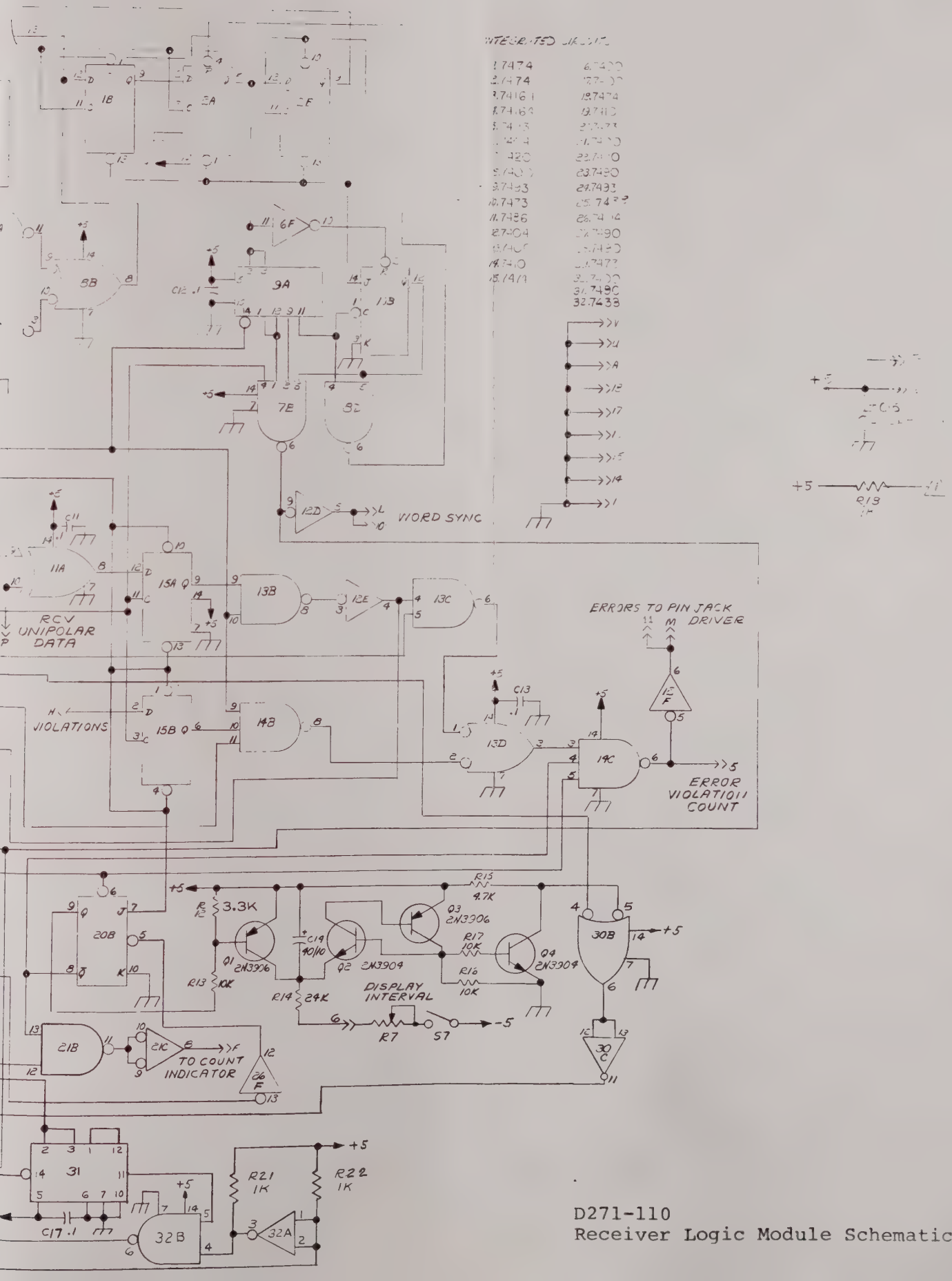
D271-113
Display Module Schematic


IC6
IC4
IC2
C1

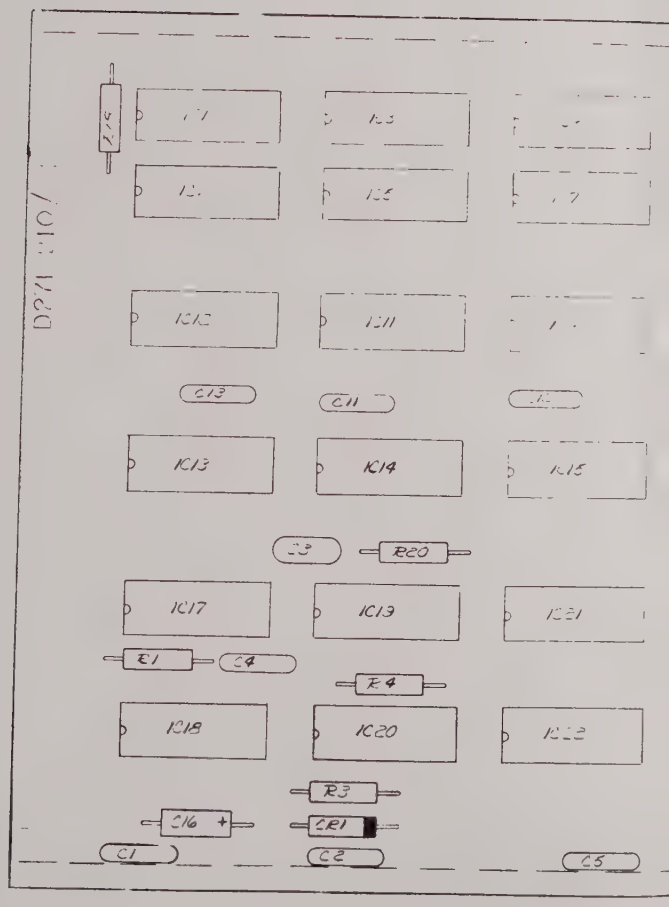


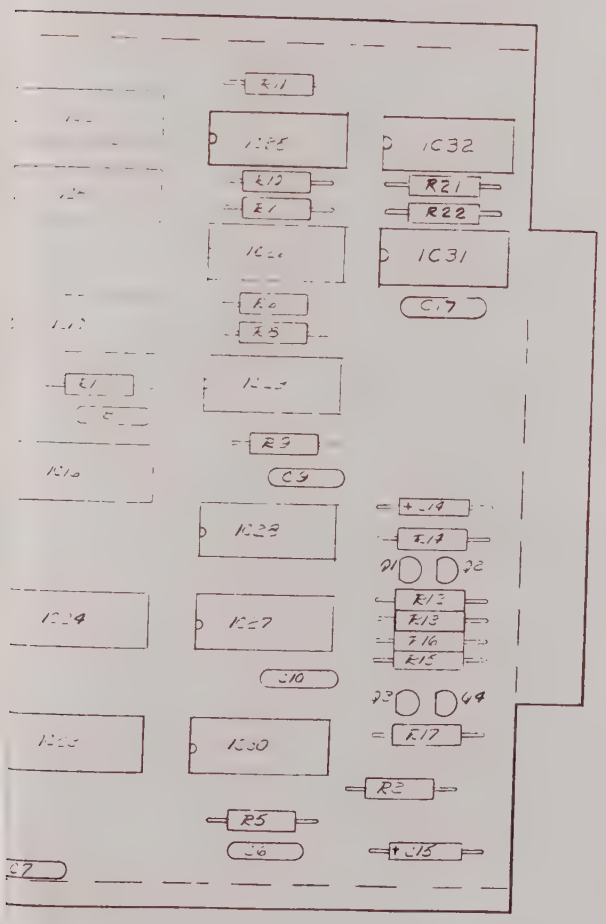
D271-213
Display Module Assembly


R I CLOCK
110 SYNC. INDICATOR
SYNC MODE
MANUAL
AUTO
S4
RESET/RESYNC SWITCH
RESET ERROR E COUNTER
OVERFLOW FROM ERROR COUNTER
J OVER-FLOW IND.
LOST SYNC. INDICATOR
ERRORS
VIOLATIONS
S6 COUNT INTERVAL

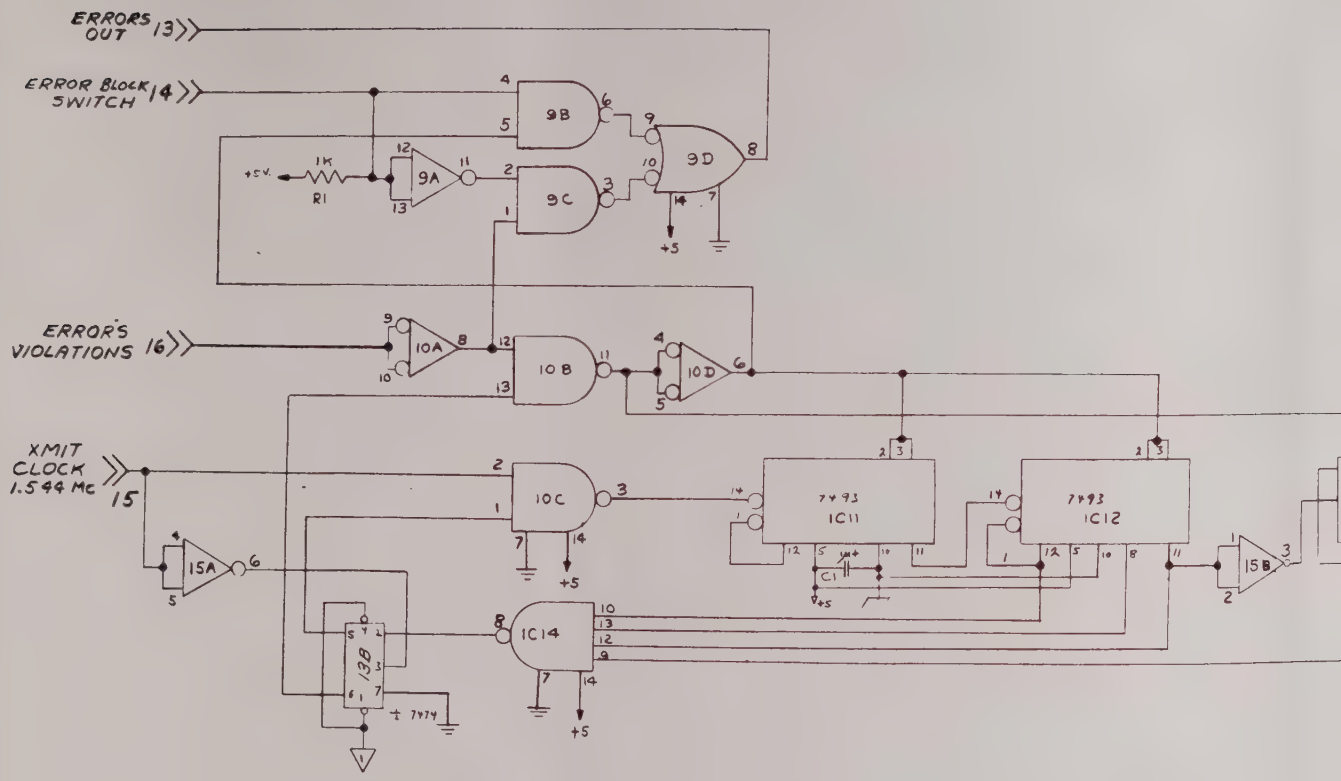


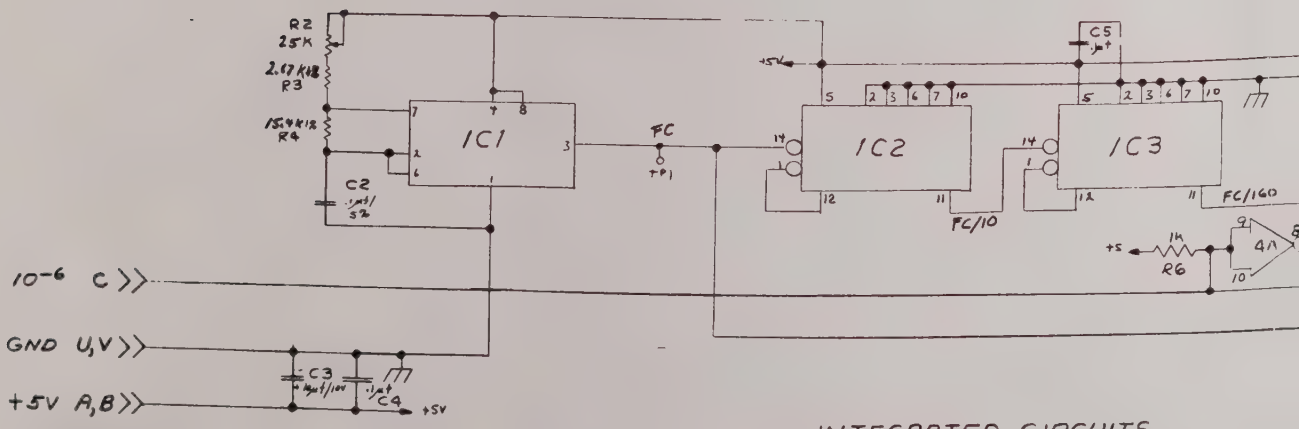
D271-110
Receiver Logic Module Schematic


D271 :10/ :: 120
R19
IC7
IC8
IC12
IC5
IC7
IC10
IC11
C13
C11
IC13
IC14
IC15
C9
R20
IC17
IC16
IC21
R1
C4
R4
IC18
IC20
IC22
R3
C16 +
CR1
C1
C2
C5



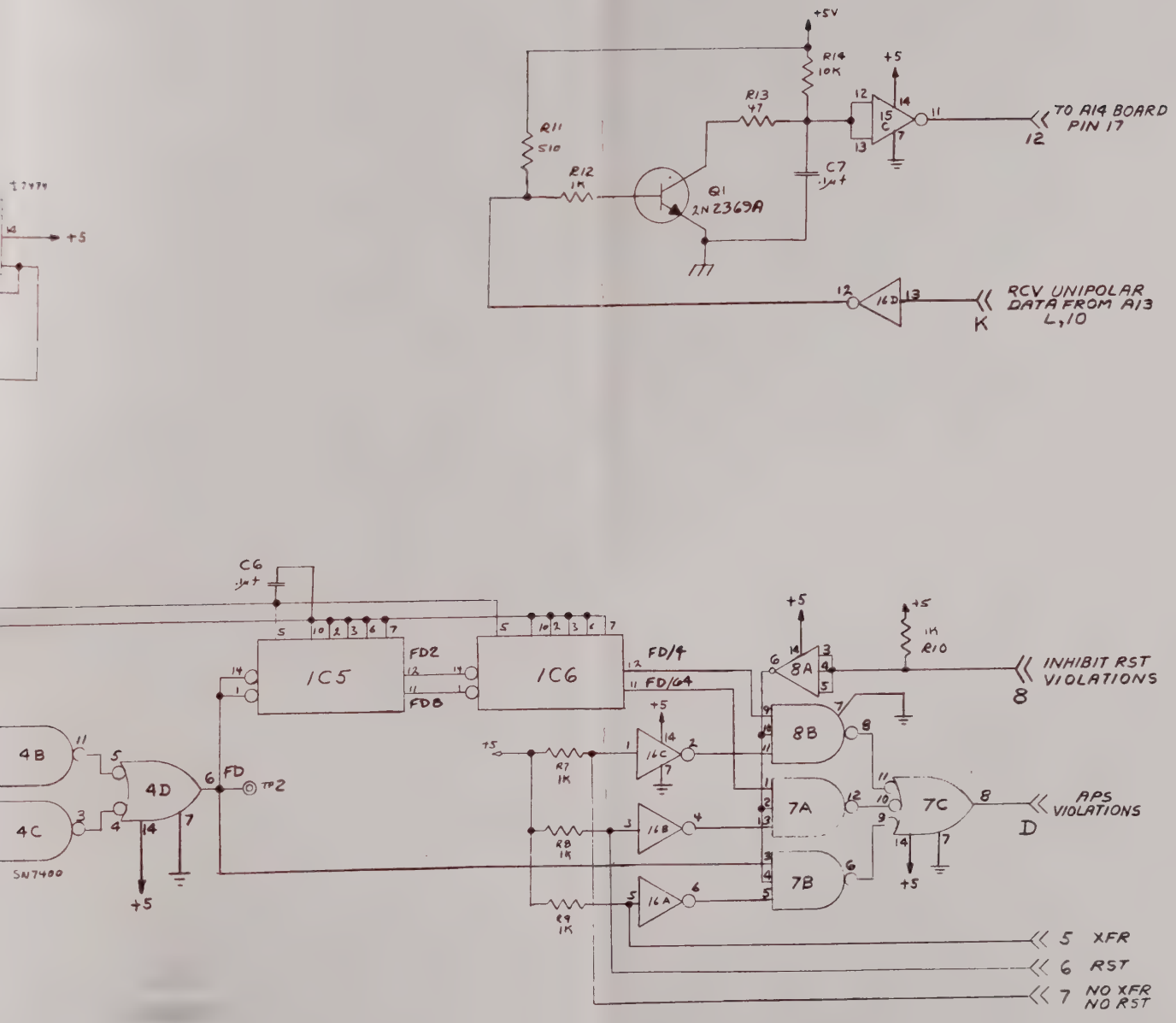
D271-210
Receiver Logic Module Assembly





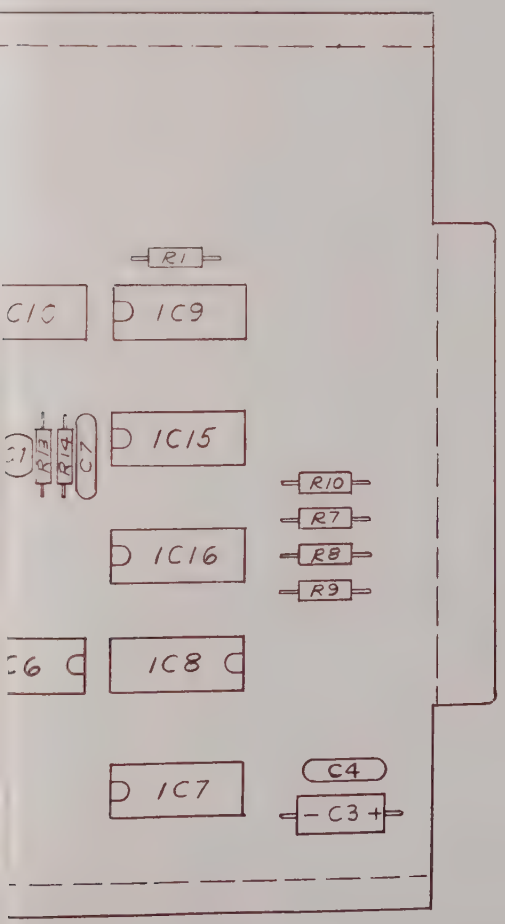
INTEGRATED CIRCUITS

1. NE555V
2. 7490
3. 7493
4. 7400
5. 7493
6. 7493
7. 7410
8. 7410
9. 7400
10. 7400
11. 7493
12. 7493
13. 7474
14. 7420
15. 7400
16. 7404

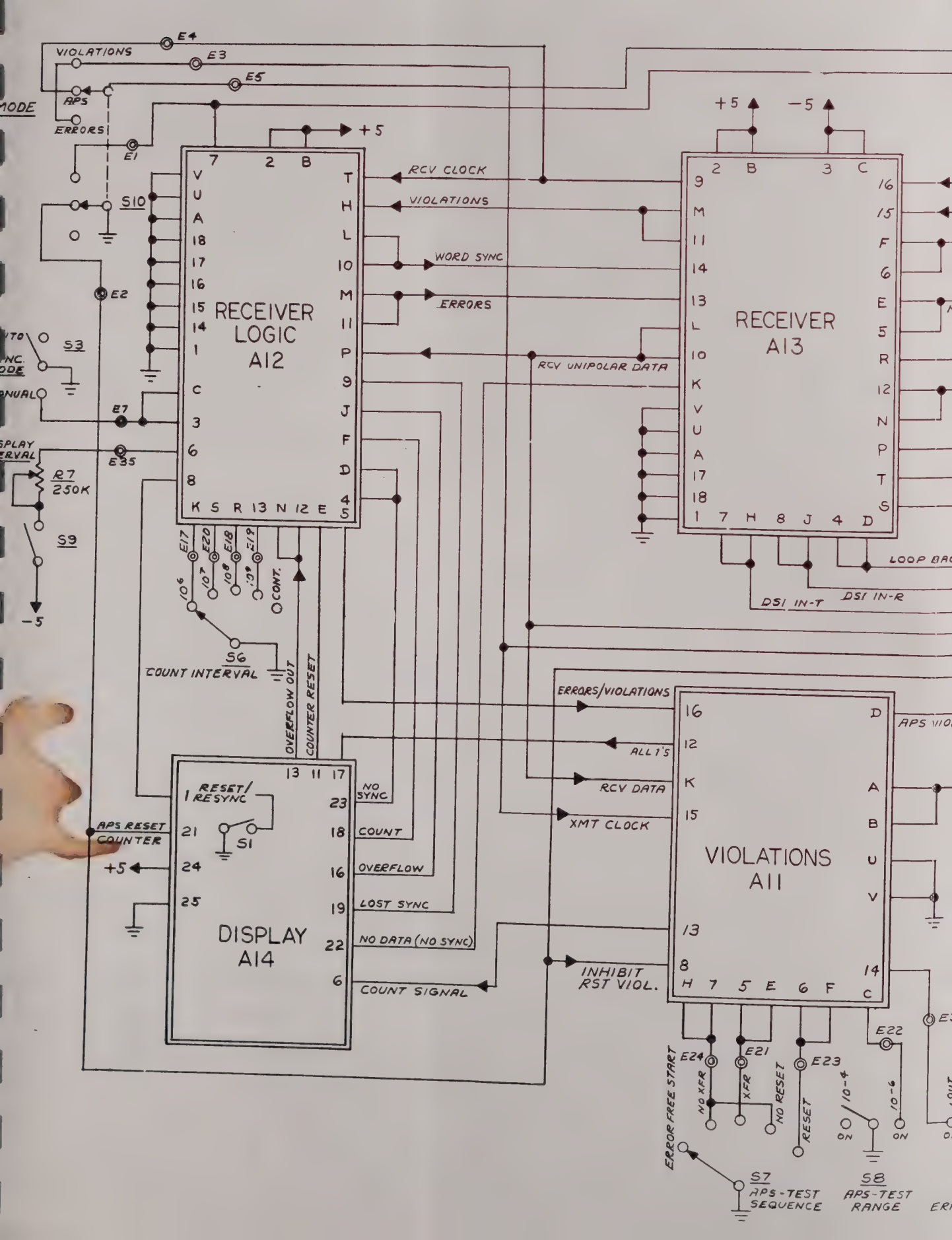


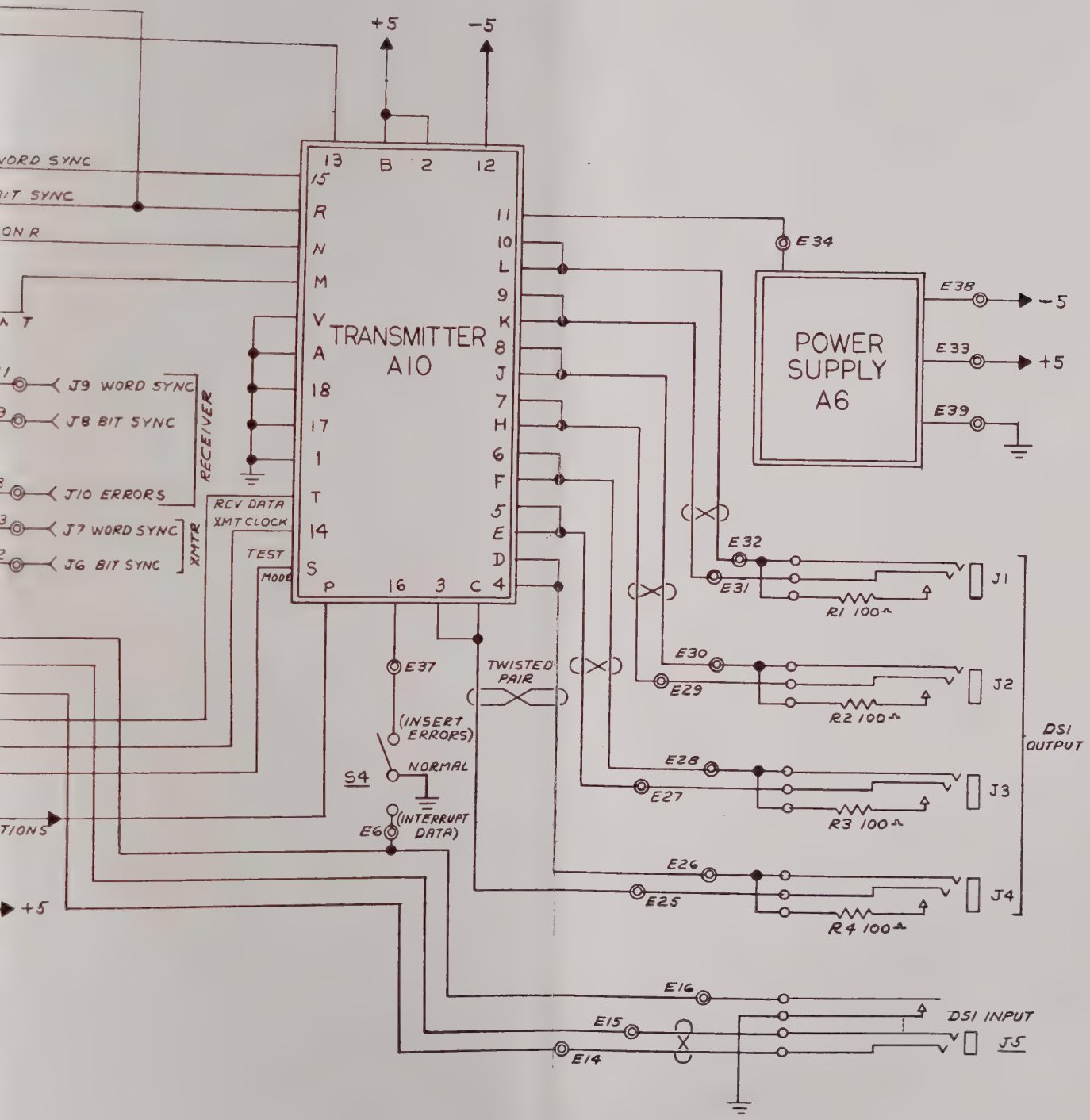
D271-117
Violations Schematic

D271-217/
C1
IC12
IC11
IC14
R5
IC13
C2
C5
C6
IC10
IC2
IC3
IC5
R2
R3
R6
R4
IC4

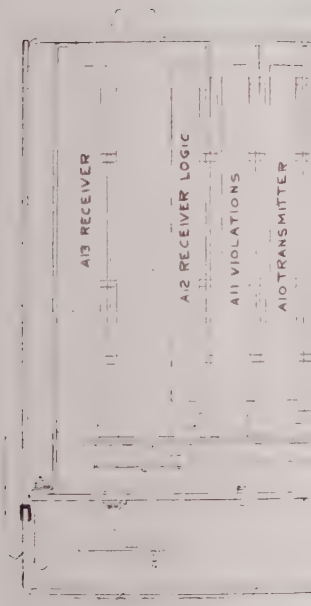


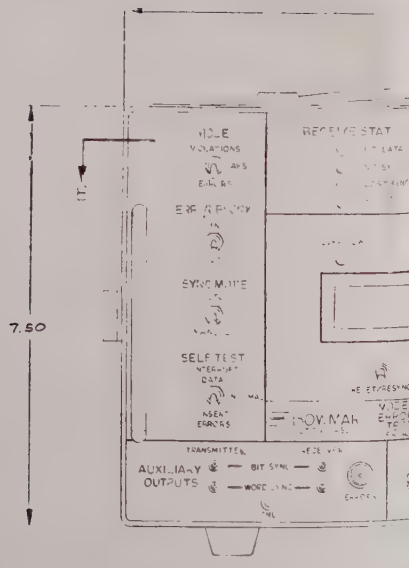
D271-217
Violations Assembly


VIOLATIONS
E4
E3
E5
APS
ERRORS
MODE
E1
+5
S10
E2
S3
E7
E35
R7
250K
S9
-5
RECEIVER
LOGIC
A12
RCV CLOCK
VIOLATIONS
WORD SYNC
ERRORS
RCV UNIPOLAR DATA
RECEIVER
A13
+5
-5
LOOP BA
DSI IN-T
DSI IN-R
E17
E20
E18
E19
CONT.
S6
COUNT INTERVAL
OVERFLOW OUT
COUNTER RESET
ERRORS/VIOLATIONS
ALL 1'S
RCV DATA
XMT CLOCK
VIOLATIONS
A11
APS VIO
INHIBIT
RST VIOL.
RESET/
RESYNC
S1
APS RESET
COUNTER
+5
DISPLAY
A14
NO
SYNC
COUNT
OVERFLOW
LOST SYNC
NO DATA (NO SYNC)
COUNT SIGNAL
E22
E24
E21
E23
NO XFR
XFR
NO RESET
RESET
10-4
10-6
ON
ON
ERROR FREE START
S7
APS-TEST
SEQUENCE
S8
APS-TEST
RANGE

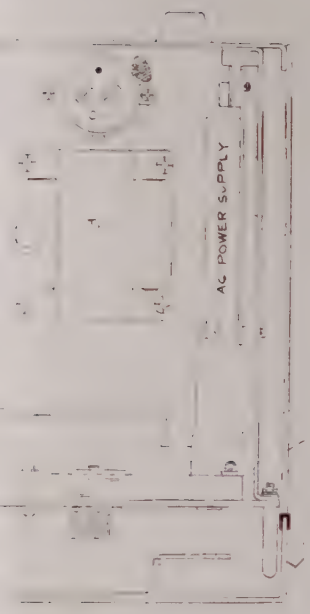


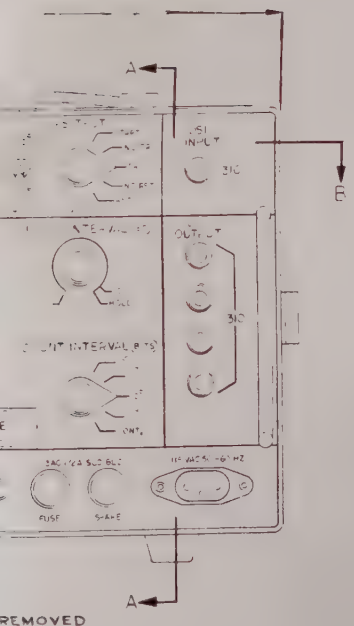
D271-114
Main Schematic

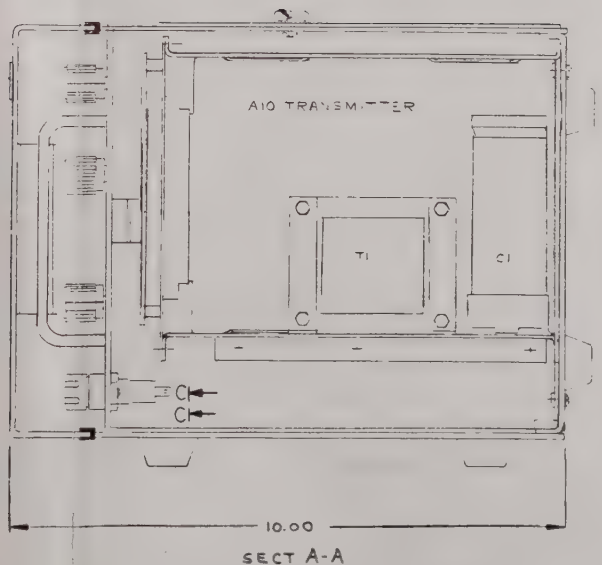




SHOWN WITH COV







SECT A-A

E271-227
Main Assembly

CHAPTER 7

PARTS AND MANUFACTURERS

Items listed herein are electrical and circuit components. They are grouped under the title of associated modules. Each part is itemized by REF. DES. (Reference Designation) and described according to title, values, manufacturer, and manufacturer's identification number. Exception to providing manufacturer identification is taken where the part is standardized RETMA. Any manufacturer registered for RETMA parts will be acceptable.

A second list gives manufacturer's names, for convenience in locating specific components or related information.

REF. DES.	COMPONENT DESCRIPTION	COMPONENT MANUFACTURER	PART NO.
DISPLAY P.C. BOARD A14 (271-213)			
IC1, 3, 5	Integrated Circuit TTL		7447A
IC2, 4, 6	Integrated Circuit TTL		7490
IC7, 8	Integrated Circuit TTL		7438
LED1, 2, 3	7 Segment LED	G.I. Dialco	MAN-72 or 745-0017
R1-R22, R24-R28	Resistor, 150, 1/4W, 5%		RC07GF151J
R30, 29	Resistor, 1K, 1/4W, 5%		
C1	Capacitor, 0.1uf, Disc., 16V	Centralab	UK-16-104
DS1, DS3-DS7	LED	Fairchild	FLV-110 or Equiv.
S1	Switch	C & K	7109SPV30CQE
POWER SUPPLY BOARD ASSEMBLY (271-204)			
CR1,2,3,4,9,11	Diode Rectifier 1 amp		1N4003
CR8, 10	Diode Rectifier 3 amp		1N4720
CR5, 7, 12	Diode		1N4148
CR6, 13	Diode, Zener		1N749A
Q1, 6	Transistor, With Mica Insulator & Shoulder Washer	T.I.	TIP-29
Q9	Transistor, With Mica Insulator & Shoulder Washer	T.I.	TIP-30
Q3	Transistor, With Mica Insulator & Shoulder Washer	T.I.	TIP-33
Q2, 4, 5	Transistor, NPN		2N3904
Q7, 8	Transistor PNP		2N3906
R2	Resistor, 4.7K, 1/2W, 5%		RC20GF472J
R4, 9, 10	Resistor, 270, 1/2W, 5%		RC20GF271J
R3, 8	Resistor, 10, 1/2W, 5%		RC20GF100J
R1, 7	Resistor, 27K, 1/2W, 5%		RC20GF273J
R5	Resistor, 300, 1/2W, 5%		RC20GF301J
R6	Potentiometer, 100 ohm	Beckman or Bourns	89PR100 or 3006P-1-101

REF. DES.	COMPONENT DESCRIPTION	COMPONENT MANUFACTURER	PART NO.
POWER SUPPLY BOARD ASSEMBLY (271-204) (Con't)			
2, 4	Capacitor, 47uf, 50V or 50uf, 50V	Capar or Sprague	CAE-E47M50V or TE-1307E
C1, 3	Capacitor, 22uf, 50V or 25uf, 50V	Capar or Sprague	CAE-E22M50V or TE-1305E
C9, 12	Capacitor, 22uf, 16V or 20 uf, 16V	Capar or Sprague	CAE-E22M16V TE-1157E
C8	Capacitor, .1uf, 16V	Centralab	UK-16-104
C10	Capacitor, 470uf, 25V	Capar or Siemens	CAE-E470M25V or 470/25/82006
C7, 11	Capacitor, 100pf	CDE	CD10FD101JGF03
C6	Capacitor, 270pf	CDE	CD10FE271JGF03
CHASSIS, ELECTRICAL ASSEMBLY (271-215)			
A11	Violations Assembly	Bowmar/ALI	D271-217
A12	Receiver Logic Assembly	Bowmar/ALI	D271-210
A13	Receiver Assembly	Bowmar/ALI	D271-212-1
A10	Transmitter Assembly	Bowmar/ALI	D271-211
A15	Interconnection Board Assembly	Bowmar/ALI	C271-214
A14	Display Board Assembly	Bowmar/ALI	C271-213
A6	Power Supply Assembly	Bowmar/ALI	C271-204
C1	Capacitor, Electrolytic, 8700uf, 25 VDC	Mepco/Electra or Sprague	3186BE872U025AM or 36D822G025AC2A
T1	Transformer	Bowmar/ALI	B6218
RECEIVER LOGIC P.C. BOARD A12 (271-210)			
IC8,13,16,17,21,30	Integrated Circuit TTL		7400
IC6, 12, 26	Integrated Circuit TTL		7404
IC14, 19	Integrated Circuit TTL		7410
IC7	Integrated Circuit TTL		7420
IC10, 20, 29	Integrated Circuit TTL		7473
IC1, 2, 15, 18	Integrated Circuit TTL		7474
IC11	Integrated Circuit TTL		7486
IC22,23,27,28,31	Integrated Circuit TTL		7490

REF. DES.	COMPONENT DESCRIPTION	COMPONENT MANUFACTURER	PART NO.
RECEIVER LOGIC P.C. BOARD A12 (271-210) (Con't)			
IC5, 9, 24	Integrated Circuit TTL		7493
IC3, 4	Integrated Circuit TTL		74164
IC25, 32	Integrated Circuit TTL		7438
Q2, 4	Transistor NPN		2N3904
Q1, 3	Transistor PNP		2N3906
CR1	Diode		1N4148
R6	Resistor, 470, 1/4W, 5%		RC07GF471J
R1,2,4,5,7,8,9,10, R11,18,19,21,22	Resistor, 1K, 1/4W, 5%		RC07GF102J
R15	Resistor, 4.7K, 1/4W, 5%		RC07GF472J
R3,13,16,20	Resistor, 10K, 1/4W, 5%		RC07GF103J
R14	Resistor, 24K, 1/4W, 5%		RC07GF243J
R17	Resistor, 2K, 1/4W, 5%		RC07GF202J
R12	Resistor, 3.3K, 1/4W, 5%		RC07GF332J
C1,2,4,5,6,7,8,9,10, C11,12,13,17	Capacitor, 0.1uf, Disc.	Centralab	UK-16-104
C14	Capacitor, 40uf, 10V or 39uf, 10	Sprague	150D406X9010B2 or 150D396X9010B2
C15	Capacitor, 10uf, 16V	Capar or Sprague	CAE-E10M16V or TE-1155E
C16	Capacitor, 22uf, 25V or 20uf, 16V	Mepco/Electra or CDE	ET220X025A3 or 3071CD220T025B or NLW-20-16
C3	Capacitor, .001uf, Disc.	Centralab	DD-102
TRANSMITTER P.C. BOARD A10 (271-211)			
IC11,14,16,18,19,22	Integrated Circuit TTL		7400
IC13, 20	Integrated Circuit TTL		7404
IC9, 10	Integrated Circuit TTL		7420
IC7, 15, 17	Integrated Circuit TTL		7473
IC1, 4, 12, 24	Integrated Circuit TTL		7474
IC5, 6, 21	Integrated Circuit TTL		7493
IC2, 3	Integrated Circuit TTL		74164
IC8, 23	Integrated Circuit TTL		7486

REF. DES.	COMPONENT DESCRIPTION	COMPONENT MANUFACTURER	PART NO.
TRANSMITTER P.C. BOARD A10 (271-211) (Con't)			
Q4,5,6,7,8	Transistor NPN		2N2369A
Q1, 3	Transistor (Not MPS)		2N3904
Q2	Transistor (Not MPS)		2N3906
T1	Pulse Transformer	Pulse Engineering or	PE-5762
		AIE	318-0433
L1	Coil, 47uh	Lenox Fugle	NR47 (LF47)
X1	Crystal, 3.088 MHz	Bowmar/ALI	B6221
R10	Resistor, 10K, 1/4W, 5%		RC07GF103J
R13, 15, 17, 19	Resistor, 6.2K, 1/4W, 5%		RC07GF622J
R14, 16, 18, 20	Resistor, 360, 1/4W, 5%		RC07GF361J
R12,33,9,34,35,36,37	Resistor, 1K, 1/4W, 5%		RC07GF102J
R11	Resistor, 4.7K, 1/4W, 5%		RC07GF472J
R23-30	Resistor, 51, 1/4W, 5%		RC07GF510J
R31, 32	Resistor, 62, 1/4W, 5%		RC07GF620J
R22	Resistor, 270, 1/4W, 5%		RC07GF271J
R21	Resistor, 680, 1/4W, 5%		RC07GF681J
R6	Resistor, 324, 1/8W, 1%		RN60C3240F
R7	Resistor, 357, 1/8W, 1%		RN60C3570F
R8	Resistor, 536, 1/8W, 1%		RN60C5360F
R5	Resistor, 750, 1/8W, 1%		RN60C7500F
R4	Resistor, 1.33K, 1/8W, 1%		RN60C1331F
R3	Resistor, 3.83K, 1/8W, 1%		RN60C3831F
C9	Capacitor, 0.01uf	Centralab	UK-16-103
C4,7,8,12,14,15,16 C17,18,19,22	Capacitor, 0.1uf	Centralab	UK-16-104
C10	Capacitor, 220pf	CDE	CD10FD221J03
C13	Capacitor, 200pf	CDE	CD10FD201J03
C23	Capacitor, 10pf, ±5% N1500	RMC	Type C RMC 75
C11, 20, 21	Capacitor, 10uf, 16V	Capar or Sprague	CAE-E10M16V or TE-1155E
C1	Capacitor, Variable, 1-18pf	Erie	567-013
C3	Capacitor, 30pf, ± 5%, N2200	RMC	Type C RMC 75

REF. DES.	COMPONENT DESCRIPTION	COMPONENT MANUFACTURER	PART NO.
TRANSMITTER P.C. BOARD A10 (271-211) (Con't)			
C5, 6	Capacitor, 75pf	CDE	CD10ED750J03
C2 (Selected)	Capacitor, 10pf, ± 5%, N1500	RMC	Type C RMC 75
	20pf, ± 5%, N1500	RMC	Type C RMC 75
	30pf, ± 5%, N1500	RMC	Type C RMC 75
	39pf, ± 5%, N1500	RMC	Type C RMC 75
CR1	Diode		1N4148
E1, 2	Solder Terminal	Cambion	2027-2
RECEIVER P.C. BOARD A13 (271-212)			
C26	Capacitor, 3900pf	CDE	CD19FD392J
C12	Capacitor, 12pf, 5%, Mica	CDE	CM04CD120J03
C1,2,6,8,9,13,14,15, C16,17,18,19	Capacitor, 0.1uf, 16V, Disc.	Centralab	UK-16-104
C20, 21	Capacitor, 10uf, 16V	Capar or	CAE-E10M16V
		Sprague	TE-1155E
C3	Capacitor, 10uf, 10V	Sprague	150D106X9010B2
C11	Capacitor, Variable, 1-18pf	Erie	567-013
C5	Capacitor, 75pf, 5%, N030	Sprague	561CS1GAA102AJ750J
C7	Capacitor, 150pf, 5%, N150	RMC	CMRMC390150N150±5%
		or	or
		Aerovox or	D1-6AN150150±5% or
		Sprague	561CP2GAA102AL151J
C27	Capacitor, 47uf, 10V	Sprague	150D476X9010B2
C24, 25	Capacitor, 20pf, 5%	CDE	CD10ED200J03
IC9	Integrated Circuit		74123
IC3, 6	Integrated Circuit TTL		7400
IC2, 4	Integrated Circuit TTL		7473
IC1	Integrated Circuit TTL		7474
IC5, 7	Integrated Circuit Line Receiver		75107A
IC8	Transistor Array NPN	RCA	CA3083
Q2, 7, 8	Transistor (Not MPS)		2N3904
Q1	Transistor (Not MPS)		2N3906
Q9,10,11,12,13	Transistor NPN		2N2369A
CR1, 3	Diode		1N4148

REF. DES.	COMPONENT DESCRIPTION	COMPONENT MANUFACTURER	PART NO.
RECEIVER P.C. BOARD A13 (271-212) (Con't)			
R8, 9	Resistor, 140, 1/4W, 1%		RN65C1400F
R2, 3	Resistor, 18, 1/4W, 5%		RC07GF180J
R4	Resistor, 62, 1/4W, 5%		RC07GF620J
R57	Resistor, 23.7K, 1/8W, 1%		RN60C2372F
R15	Resistor, 180, 1/4W, 5%		RC07GF181J
R10,11,18,19,59,28	Resistor, 1K, 1/4W, 5%		RC07GF102J
R5, 12, 13	Resistor, 2K, 1/4W, 5%		RC07GF202J
R33,35,40,41,30	Resistor, 6.2K, 1/4W, 5%		RC07GF622J
R6, 21	Resistor, 10K, 1/4W, 5%		RC07GF103J
R1	Resistor, 24K, 1/4W, 5%		RC07GF243J
R55	Resistor, 470, 1/4W, 5%		RC07GF471J
R31,34,37,42,43	Resistor, 75, 1/2W, 5%		RC20GF750J
R56	Resistor, 6.8K, 1/4W, 5%		RC07GF682J
R54	Resistor, 22K, 1/4W, 5%		RC07GF223J
R29,32,36,38,39	Resistor, 360, 1/4W, 5%		RC07GF361J
R17, 26	Resistor, 10, 1/4W, 5%		RC07GF100J
R7	Resistor, 1.6K, 1/4W, 5%		RC07GF162J
T1	Transformer	Pulse Engineering or AIE	PE-5762 or 319-0433
K1	Reed Relay	Coto-Coil	UD-12-P1
L1	Tapped Inductor	Bowmar	B6346
L4	Inductor, 330uh	Lenox Fugle	NR-330 LF-330
L2, 3	Inductor, 100uh	Lenox Fugle	NR-100 LF-100
TP1, 2, 3, 4	Terminal, Turret	Cambion	2027-2
FRONT PANEL ASSEMBLY (271-216)			
J1, 2, 3, 4	Phone Jack	Switchcraft	MT-333B
J5	Phone Jack	Switchcraft	MT-336B
J6, 7, 8, 9	Insulated Jack	Sealectro	SKT-5BC-Gray
J11	Terminal Ground	Lundey	601TH
J10	Connector BNC	Amphenol	UG-1094-U

REF. DES.	COMPONENT DESCRIPTION	COMPONENT MANUFACTURER	PART NO.
FRONT PANEL ASSEMBLY (271-216) (Con't)			
S2, 3, 8, 11	Switch, SPDT	C & K	7101SPHZQEU11
S4	Switch, Momentary	C & K	7105SPHZQE
S6, 7	Switch, Subminiature, Rotary, 0 Index, 5 Position	Bowmar/ALI	B6439-1
S10	Switch, 3 Position	C & K	7411SPHZQE
DS1	Lamp, Glo-Dot	Industrial Devices	2150A1
XF1, XF2	3 AG Fuse Extractor Post	Littlefuse	342014A
F1, 2	3 AG Fuse, Slo-Blo, 1/2 A	Littlefuse	313500
P1	Receptacle	Switchcraft	EAC302
R7-S9	Variable Resistor & AC Switch	Bowmar/ALI	B6220-1
INTERCONNECTION BOARD ASSEMBLY A15 (271-214)			
XA10, 11, 12, 13	Double Readout Connector Printed Circuit Mtg. 18 Pins	TRW/Cinch	252-18-30-160
E1-E39	Solder Terminal	Cambion	2027-2
VIOLATIONS P.C. BOARD A11 (271-217)			
R4	Resistor, 15.4K, 1/8W, 1%		RN60C1542F
R2	Potentiometer, 25K	Bourns or Beckman	3006W-1-253 or 89W25K
R1,5,6,7,8,9,10,12	Resistor, 1K, 1/4W, 5%		RC07GF102J
R14	Resistor, 10K, 1/4W, 5%		RC07GF103J
R11	Resistor, 510, 1/4W, 5%		RC07GF511J
R13	Resistor, 47, 1/4W, 5%		RC07GF470J
R3	Resistor, 2.67K, 1/8W, 1%		RN60C2671F
C4,5,6,7,1	Capacitor, .1uf Disc.		UK-16-104
C3	Capacitor, 10uf, 10V		TAD10TA10IEC
C2	Capacitor, .1uf, 100V, 5%	TRW	X601PE
Q1	Transistor		2N2369A

REF. DES.	COMPONENT DESCRIPTION	COMPONENT MANUFACTURER	PART NO.
VIOLATIONS P.C. BOARD A11 (271-217) (Con't)			
IC4,9,10,15	Integrated Circuit TTL DIP		7400
IC11,12,6,3,5	Integrated Circuit TTL DIP		7493
IC2	Integrated Circuit TTL DIP		7490
IC7, 8	Integrated Circuit TTL DIP		7410
IC14	Integrated Circuit TTL DIP		7420
IC13	Integrated Circuit TTL DIP		7474
IC1	Timer	Signetics	NE555V
IC16	Integrated Circuit TTL DIP		7404
WIRING DIAGRAM (271-106)			
R1 - R4	Resistor, 100, 1/4W, 5%		RC07GF101J

LIST OF MANUFACTURERS

Abbreviation	Complete Name and Address
Aerovox	Aerovox, Inc. 740 Belleville Avenue New Bedford, MA 02741
AIE	AIE Division of Vernitron 701 Murfreesboro Road Nashville, TN 37210
Amphenol	Amphenol North America Division Bunker Ramo Corporation 2122 York Road Oak Brook, IL 60521
Beckman	Beckman Instruments Inc. 2500 Harbor Boulevard Fullerton, CA 92634
Bourns	Bourns Inc. 1200 Columbia Avenue Riverside, CA 92507
Bowmar/ALI	Bowmar/ALI, Inc. 531 Main Street Acton, MA 01720
C & K	C & K Components, Inc. 15 Riverdale Avenue Newton, MA 02151
CDE	Cornell-Dublier Electronics, Inc. 150 Avenue "L" Newark, NJ 07105
Cambion	Cambridge Thermionic Corporation 445 Concord Avenue Cambridge, MA 02138
Capar	Capar 110 Marcus Drive Melville, NY 11747
Centralab	Centralab, Inc. 5757 North Green Bay Avenue Milwaukee, WI 53201

Coto-Coil	Coto Corporation 65e Pavilion Avenue Providence, RI 02905
Dialco	Dialight 203 Harrison Place Brooklyn, NY 11237
Erie	Erie Technological Products P.O. Box 961 Erie, PA 16512
Fairdhild	Fairchild Semiconductor Components 464 Ellis Street Mountain View, CA 94042
G.I.	General Instruments Optoelectronics Division 3400 Hillview Avenue Palo Alto, CA 94304
Industrial Devices	Industrial Devices Inc. Edgewater, NJ 07020
Lenox Fugle	Lenox Fugle Electronics Inc. 100 Sylvania Place South Plainfield, NJ 07080
Littlefuse	Littlefuse Inc. 800 East Northwest Highway Des Plaines, IL 60016
Lundey	Lundey Associates 51 Newcomb Street Attelboro, MA 02703
Mepco/Electra	Mepco/Electra, Inc. 11468 Sorrento Valley Road San Diego, CA 92121
Pulse Engineering	Pulse Engineering, Inc. Box 12235 San Diego, CA 92112
RCA	RCA Solid State Division Route 202 Somerville, NJ 08876
RMC	Radio Materials Corporation 4242 West Bryn Mawr Avenue Chicago, IL 60646

Sealectro	Sealectro Corporation 225 Hoyt Street Mamaroneck, NY 10543
Siemens	Siemens Corporation 186 Wood Avenue South Iselin, NJ 08830
Signetics	Signetics Corporation 811 East Arques Avenue Sunnyvale, CA 94086
Sprague	Sprague Electric Company 481 Marshall Street North Adams, MA 01247
Switchcraft	Switchcraft, Inc. 5555 North Elston Avenue Chicago, IL 60630
T.I.	Texas Instruments, Inc. Box 225012 Dallas, TX 75265
TRW	TRW Capacitors 301 West O Street Ogallala, NB 69153
TRW/Cinch	TRW/Cinch Connectors 1501 Morse Avenue Elk Grove Village, IL 60007